SSD1606

Advanced information

4GS Active Matrix EPD 128 x 180 Display Driver with Controller

Appendix: IC Revision history of SSD1606 Specification

Revision	Change Items	Effective Date
1.0	Advanced information Release	11-May-11
1.1	Change ordering information	17-Oct-11

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1 GENERAL DESCRIPTION

SSD1606 is a CMOS active matrix bistable display driver with controller. It consists of 128 source outputs plus 180 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 128x180.

SSD1606 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

2 FEATURES

- Design for dot matrix type active matrix EPD display
- Resolution: 128 source outputs; 180 gate outputs; 1 VCOM; 1VBD for border
- Power supply
  - VCI: 2.4 to 3.3V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply

- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 15V to 22V;
  - VGL: -20V to -15V
  - Voltage adjustment in steps of 500mV.

- Source / VBD driving output voltage:
  - 3 levels output (VSH, VSS, VSL)
  - VSH: 10V to 17V
  - VSL: -10V to -17V
  - Voltage adjustment in steps of 500mV

- VCOM output voltage
  - -4V to 0.2V in 20mV resolution
  - 8 bits Non-volatile memory (OTP) for VCOM adjustment

- Source and gate scan direction control
- Low current deep sleep mode
- On chip display RAM of 11520 bytes [(128x180) x 2 x 2 / 8] with double display buffer
- 11 set of waveform settings can be programmed and stored in On-chip OTP
- Programmable output waveform allowing flexibility for different applications / environments.
- Built in VCOM sensing
- 8-bits Parallel (6800 & 8080), Serial peripheral interface available
- On-chip oscillator.
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage.
- I2C Single Master Interface to read external temperature sensor reading
- Available in COG package, IC thickness 250um

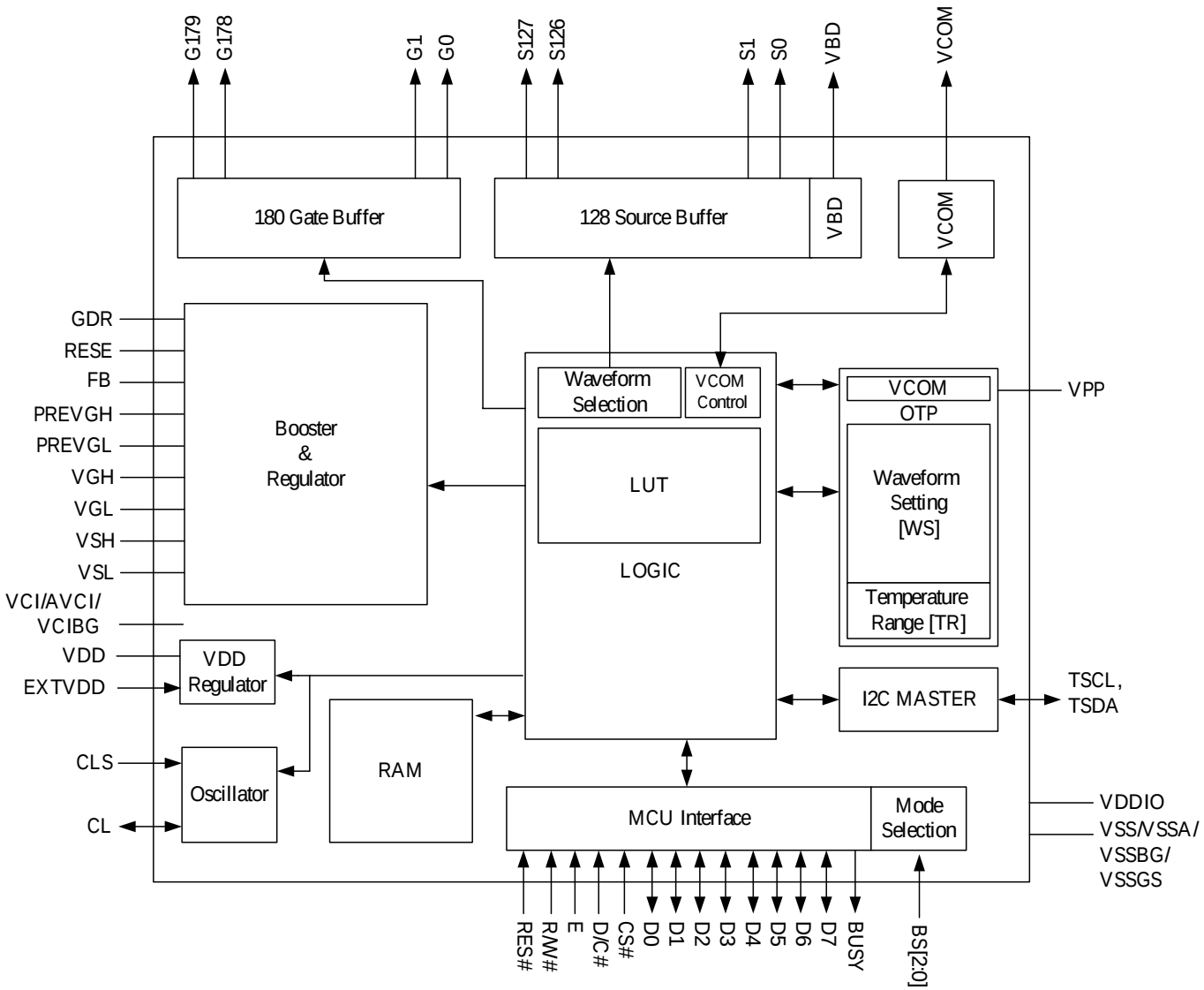
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form
SSD1606Z0	Gold bump die

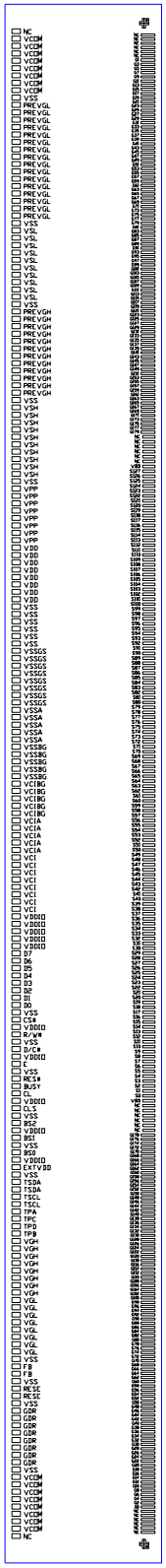
4 BLOCK DIAGRAM

Figure 4-1 : SSD1606 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1 - SSD1606Z0 Die Floor Plan (Bump face up)



Pin539

Pin205

Pin206

Die Information:

Die Size: [After sawing]

X = 12.7 +/- 0.1 mm

Y = 1.3 +/- 0.1 mm

Output pad:

Source output pad:

20x100 = 2000 μm^2

Gate output pad:

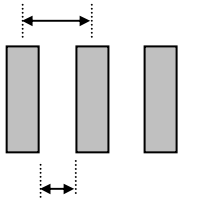
18x112 = 2016 μm^2

I/O pad:

40x70 = 2800 μm^2

Output Pad Pitch:

Output Pad Pitch: 34 um



Bump area: 2000 um^2 min

Bump gap 16μm min

Alignment Marks:

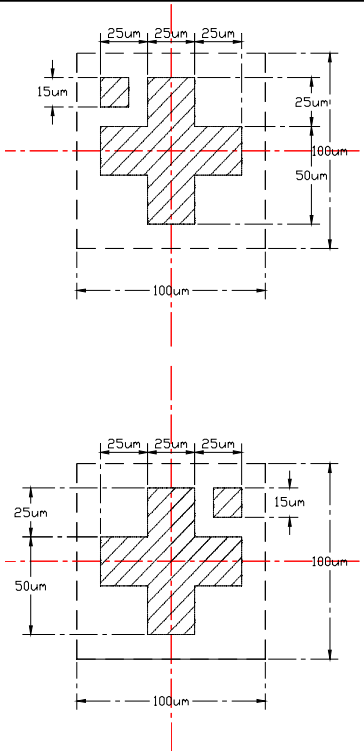


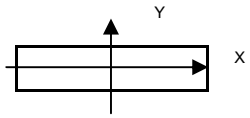
Table 5-1 : SSD1606Z0 Bump Die Pad Coordinates

PIN	NAME	X	Y
1	NC	-6120	-552
2	VCOM	-6060	-552
3	VCOM	-6000	-552
4	VCOM	-5940	-552
5	VCOM	-5880	-552
6	VCOM	-5820	-552
7	VCOM	-5760	-552
8	VCOM	-5700	-552
9	VCOM	-5640	-552
10	VSS	-5580	-552
11	PREVGL	-5520	-552
12	PREVGL	-5460	-552
13	PREVGL	-5400	-552
14	PREVGL	-5340	-552
15	PREVGL	-5280	-552
16	PREVGL	-5220	-552
17	PREVGL	-5160	-552
18	PREVGL	-5100	-552
19	PREVGL	-5040	-552
20	PREVGL	-4980	-552
21	PREVGL	-4920	-552
22	PREVGL	-4860	-552
23	PREVGL	-4800	-552
24	PREVGL	-4740	-552
25	PREVGL	-4680	-552
26	PREVGL	-4620	-552
27	VSS	-4560	-552
28	VSL	-4500	-552
29	VSL	-4440	-552
30	VSL	-4380	-552
31	VSL	-4320	-552
32	VSL	-4260	-552
33	VSL	-4200	-552
34	VSL	-4140	-552
35	VSL	-4080	-552
36	VSL	-4020	-552
37	VSL	-3960	-552
38	VSS	-3900	-552
39	PREVGH	-3840	-552
40	PREVGH	-3780	-552
41	PREVGH	-3720	-552
42	PREVGH	-3660	-552
43	PREVGH	-3600	-552
44	PREVGH	-3540	-552
45	PREVGH	-3480	-552
46	PREVGH	-3420	-552
47	PREVGH	-3360	-552
48	PREVGH	-3300	-552
49	PREVGH	-3240	-552
50	PREVGH	-3180	-552
51	VSS	-3120	-552
52	VSH	-3060	-552
53	VSH	-3000	-552
54	VSH	-2940	-552
55	VSH	-2880	-552
56	VSH	-2820	-552
57	VSH	-2760	-552
58	VSH	-2700	-552
59	VSH	-2640	-552
60	VSH	-2580	-552
61	VSH	-2520	-552
62	VSS	-2460	-552
63	VPP	-2400	-552
64	VPP	-2340	-552
65	VPP	-2280	-552
66	VPP	-2220	-552
67	VPP	-2160	-552
68	VPP	-2100	-552
69	VPP	-2040	-552
70	VPP	-1980	-552
71	VDD	-1920	-552
72	VDD	-1860	-552
73	VDD	-1800	-552
74	VDD	-1740	-552
75	VDD	-1680	-552
76	VDD	-1620	-552
77	VDD	-1560	-552
78	VDD	-1500	-552
79	VSS	-1440	-552
80	VSS	-1380	-552
81	VSS	-1320	-552
82	VSS	-1260	-552
83	VSS	-1200	-552
84	VSS	-1140	-552
85	VSSGS	-1080	-552
86	VSSGS	-1020	-552
87	VSSGS	-960	-552
88	VSSGS	-900	-552
89	VSSGS	-840	-552
90	VSSGS	-780	-552
91	VSSGS	-720	-552
92	VSSGS	-660	-552
93	VSSA	-600	-552
94	VSSA	-540	-552
95	VSSA	-480	-552
96	VSSA	-420	-552
97	VSSA	-360	-552
98	VSSBG	-300	-552
99	VSSBG	-240	-552
100	VSSBG	-180	-552
101	VSSBG	-120	-552
102	VSSBG	-60	-552
103	VCIBG	0	-552
104	VCIBG	60	-552
105	VCIBG	120	-552
106	VCIBG	180	-552
107	VCIBG	240	-552
108	VCIA	300	-552
109	VCIA	360	-552
110	VCIA	420	-552
111	VCIA	480	-552
112	VCIA	540	-552
113	VCI	600	-552
114	VCI	660	-552
115	VCI	720	-552
116	VCI	780	-552
117	VCI	840	-552
118	VCI	900	-552
119	VCI	960	-552
120	VCI	1020	-552
121	VDDIO	1080	-552
122	VDDIO	1140	-552
123	VDDIO	1200	-552
124	VDDIO	1260	-552
125	VDDIO	1320	-552
126	D7	1380	-552
127	D6	1440	-552
128	D5	1500	-552
129	D4	1560	-552
130	D3	1620	-552
131	D2	1680	-552
132	D1	1740	-552
133	D0	1800	-552
134	VSS	1860	-552
135	CS#	1920	-552
136	VDDIO	1980	-552
137	R/W#	2040	-552
138	VSS	2100	-552
139	D/C#	2160	-552
140	VDDIO	2220	-552
141	E	2280	-552
142	VSS	2340	-552
143	RES#	2400	-552
144	BUSY	2460	-552
145	CL	2520	-552
146	VDDIO	2580	-552
147	CLS	2640	-552
148	VSS	2700	-552
149	BS2	2760	-552
150	VDDIO	2820	-552
151	BS1	2880	-552
152	VSS	2940	-552
153	BS0	3000	-552
154	VDDIO	3060	-552
155	EXTVDD	3120	-552
156	VSS	3180	-552
157	TSDA	3240	-552
158	TSDA	3300	-552
159	TSCL	3360	-552
160	TSCL	3420	-552
161	TPA	3480	-552
162	TPC	3540	-552
163	TPD	3600	-552
164	TPB	3660	-552
165	VGH	3720	-552
166	VGH	3780	-552
167	VGH	3840	-552
168	VGH	3900	-552
169	VGH	3960	-552
170	VGH	4020	-552
171	VGH	4080	-552
172	VGH	4140	-552
173	VGL	4200	-552
174	VGL	4260	-552
175	VGL	4320	-552
176	VGL	4380	-552
177	VGL	4440	-552
178	VGL	4500	-552
179	VGL	4560	-552
180	VGL	4620	-552
181	VSS	4680	-552
182	FB	4740	-552
183	FB	4800	-552
184	VSS	4860	-552
185	RESE	4920	-552
186	RESE	4980	-552
187	VSS	5040	-552
188	GDR	5100	-552
189	GDR	5160	-552
190	GDR	5220	-552
191	GDR	5280	-552
192	GDR	5340	-552
193	GDR	5400	-552
194	GDR	5460	-552
195	GDR	5520	-552
196	VSS	5580	-552
197	VCOM	5640	-552
198	VCOM	5700	-552
199	VCOM	5760	-552
200	VCOM	5820	-552
201	VCOM	5880	-552
202	VCOM	5940	-552
203	VCOM	6000	-552
204	VCOM	6060	-552
205	NC	6120	-552
206	NC	6089	531
207	NC	6055	531
208	NC	6021	531
209	NC	5987	531
210	NC	5953	531
211	NC	5919	531
212	G0	5885	531
213	G2	5851	531
214	G4	5817	531
215	G6	5783	531
216	G8	5749	531
217	G10	5715	531
218	G12	5681	531
219	G14	5647	531
220	G16	5613	531
221	G18	5579	531
222	G20	5545	531
223	G22	5511	531
224	G24	5477	531
225	G26	5443	531
226	G28	5409	531
227	G30	5375	531
228	G32	5341	531
229	G34	5307	531
230	G36	5273	531
231	G38	5239	531
232	G40	5205	531
233	G42	5171	531
234	G44	5137	531
235	G46	5103	531
236	G48	5069	531
237	G50	5035	531
238	G52	5001	531
239	G54	4967	531
240	G56	4933	531
241	G58	4899	531
242	G60	4865	531
243	G62	4831	531
244	G64	4797	531
245	G66	4763	531
246	G68	4729	531
247	G70	4695	531
248	G72	4661	531
249	G74	4627	531
250	G76	4593	531
251	G78	4559	531
252	G80	4525	531
253	G82	4491	531
254	G84	4457	531
255	G86	4423	531
256	G88	4389	531
257	G90	4355	531
258	G92	4321	531
259	G94	4287	531
260	G96	4253	531
261	G98	4219	531
262	G100	4185	531
263	G102	4151	531
264	G104	4117	531
265	G106	4083	531
266	G108	4049	531
267	G110	4015	531
268	G112	3981	531
269	G114	3947	531
270	G116	3913	531
271	G118	3879	531
272	G120	3845	531
273	G122	3811	531
274	G124	3777	531
275	G126	3743	531
276	G128	3709	531
277	G130	3675	531
278	G132	3641	531
279	G134	3607	531
280	G136	3573	531
281	G138	3539	531
282	G140	3505	531
283	G142	3471	531
284	G144	3437	531
285	G146	3403	531
286	G148	3369	531
287	G150	3335	531
288	G152	3301	531
289	G154	3267	531
290	G156	3233	531
291	G158	3199	531
292	G160	3165	531
293	G162	3131	531
294	G164	3097	531
295	G166	3063	531
296	G168	3029	531
297	G170	2995	531
298	G172	2961	531
299	G174	2927	531
300	G176	2893	531
301	G178	2859	531
302	NC	2820	537
303	NC	2780	537
304	NC	2740	537
305	NC	2700	537
306	NC	2660	537
307	NC	2620	537
308	VBD	2580	537
309	S0	2540	537
310	S1	2500	537
311	S2	2460	537
312	S3	2420	537
313	S4	2380	537
314	S5	2340	537
315	S6	2300	537
316	S7	2260	537
317	S8	2220	537
318	S9	2180	537
319	S10	2140	537
320	S11	2100	537

PIN	NAME	X	Y
321	S12	2060	537
322	S13	2020	537
323	S14	1980	537
324	S15	1940	537
325	S16	1900	537
326	S17	1860	537
327	S18	1820	537
328	S19	1780	537
329	S20	1740	537
330	S21	1700	537
331	S22	1660	537
332	S23	1620	537
333	S24	1580	537
334	S25	1540	537
335	S26	1500	537
336	S27	1460	537
337	S28	1420	537
338	S29	1380	537
339	S30	1340	537
340	S31	1300	537
341	S32	1260	537
342	S33	1220	537
343	S34	1180	537
344	S35	1140	537
345	S36	1100	537
346	S37	1060	537
347	S38	1020	537
348	S39	980	537
349	S40	940	537
350	S41	900	537
351	S42	860	537
352	S43	820	537
353	S44	780	537
354	S45	740	537
355	S46	700	537
356	S47	660	537
357	S48	620	537
358	S49	580	537
359	S50	540	537
360	S51	500	537
361	S52	460	537
362	S53	420	537
363	S54	380	537
364	S55	340	537
365	S56	300	537
366	S57	260	537
367	S58	220	537
368	S59	180	537
369	S60	140	537
370	S61	100	537
371	S62	60	537
372	S63	20	537
373	S64	-20	537
374	S65	-60	537
375	S66	-100	537
376	S67	-140	537
377	S68	-180	537
378	S69	-220	537
379	S70	-260	537
380	S71	-300	537
381	S72	-340	537
382	S73	-380	537
383	S74	-420	537
384	S75	-460	537
385	S76	-500	537
386	S77	-540	537
387	S78	-580	537
388	S79	-620	537
389	S80	-660	537
390	S81	-700	537
391	S82	-740	537
392	S83	-780	537
393	S84	-820	537
394	S85	-860	537
395	S86	-900	537
396	S87	-940	537
397	S88	-980	537
398	S89	-1020	537
399	S90	-1060	537
400	S91	-1100	537

PIN	NAME	X	Y
401	S92	-1140	537
402	S93	-1180	537
403	S94	-1220	537
404	S95	-1260	537
405	S96	-1300	537
406	S97	-1340	537
407	S98	-1380	537
408	S99	-1420	537
409	S100	-1460	537
410	S101	-1500	537
411	S102	-1540	537
412	S103	-1580	537
413	S104	-1620	537
414	S105	-1660	537
415	S106	-1700	537
416	S107	-1740	537
417	S108	-1780	537
418	S109	-1820	537
419	S110	-1860	537
420	S111	-1900	537
421	S112	-1940	537
422	S113	-1980	537
423	S114	-2020	537
424	S115	-2060	537
425	S116	-2100	537
426	S117	-2140	537
427	S118	-2180	537
428	S119	-2220	537
429	S120	-2260	537
430	S121	-2300	537
431	S122	-2340	537
432	S123	-2380	537
433	S124	-2420	537
434	S125	-2460	537
435	S126	-2500	537
436	S127	-2540	537
437	VBD	-2580	537
438	NC	-2620	537
439	NC	-2660	537
440	NC	-2700	537
441	NC	-2740	537
442	NC	-2780	537
443	NC	-2820	537
444	G179	-2859	531
445	G177	-2893	531
446	G175	-2927	531
447	G173	-2961	531
448	G171	-2995	531
449	G169	-3029	531
450	G167	-3063	531
451	G165	-3097	531
452	G163	-3131	531
453	G161	-3165	531
454	G159	-3199	531
455	G157	-3233	531
456	G155	-3267	531
457	G153	-3301	531
458	G151	-3335	531
459	G149	-3369	531
460	G147	-3403	531
461	G145	-3437	531
462	G143	-3471	531
463	G141	-3505	531
464	G139	-3539	531
465	G137	-3573	531
466	G135	-3607	531
467	G133	-3641	531
468	G131	-3675	531
469	G129	-3709	531
470	G127	-3743	531
471	G125	-3777	531
472	G123	-3811	531
473	G121	-3845	531
474	G119	-3879	531
475	G117	-3913	531
476	G115	-3947	531
477	G113	-3981	531
478	G111	-4015	531
479	G109	-4049	531
480	G107	-4083	531

PIN	NAME	X	Y
481	G105	-4117	531
482	G103	-4151	531
483	G101	-4185	531
484	G99	-4219	531
485	G97	-4253	531
486	G95	-4287	531
487	G93	-4321	531
488	G91	-4355	531
489	G89	-4389	531
490	G87	-4423	531
491	G85	-4457	531
492	G83	-4491	531
493	G81	-4525	531
494	G79	-4559	531
495	G77	-4593	531
496	G75	-4627	531
497	G73	-4661	531
498	G71	-4695	531
499	G69	-4729	531
500	G67	-4763	531
501	G65	-4797	531
502	G63	-4831	531
503	G61	-4865	531
504	G59	-4899	531
505	G57	-4933	531
506	G55	-4967	531
507	G53	-5001	531
508	G51	-5035	531
509	G49	-5069	531
510	G47	-5103	531
511	G45	-5137	531
512	G43	-5171	531
513	G41	-5205	531
514	G39	-5239	531
515	G37	-5273	531
516	G35	-5307	531
517	G33	-5341	531
518	G31	-5375	531
519	G29	-5409	531
520	G27	-5443	531
521	G25	-5477	531
522	G23	-5511	531
523	G21	-5545	531
524	G19	-5579	531
525	G17	-5613	531
526	G15	-5647	531
527	G13	-5681	531
528	G11	-5715	531
529	G9	-5749	531
530	G7	-5783	531
531	G5	-5817	531
532	G3	-5851	531
533	G1	-5885	531
534	NC	-5919	531
535	NC	-5953	531
536	NC	-5987	531
537	NC	-6021	531
538	NC	-6055	531
539	NC	-6089	531



Pad 1,2,3,...>> 205
Gold Bumps face up

Unit in um			
Die height		250 +/- 25	
Bump height		12	
Bump size		X	Y
Pad	1-205	40	70
Pad	206-301	18	112
Pad	302-443	20	100
Pad	444-539	18	112
Alignment mark		X	Y
	'+ shape	6185	498
	+' shape	-6185	498

6 Pin Description

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to V_{SS}, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
Input power					
VCI	P	Power Supply	Power Supply	Power Supply for the chip	-
VCIA	P	Power Supply	Power Supply	Power input for the chip, Connected with VCI	-
VCIBG	P	Power Supply	Power Supply	Power input for the chip (Reference), Connected with VCI	-
VDDIO	P	Power Supply	Power for interface logic pins	Power Supply for the Interface It should be connected with VCI	-
VDD	P	Capacitor	Regulator output	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances.	-
EXTVDD	I	VDDIO/VSS	Reserve for Testing	This pin is VDD regulator enable pin. It should be connected with VSS.	-
VSS	P	VSS	GND	Ground (Digital)	-
VSSA	P	VSS	GND	Ground (Analog) It should be connected with VSS.	-
VSSBG	P	VSS	GND	Ground (Reference) Connected with VSS	-
VSSGS	P	VSS	GND	Ground (Output) Connected with VSS	-
VPP	P	Power Supply	OTP power	Power Supply for OTP Programming	Open
Digital I/O					
D [7:0]	I/O	MPU	Data Bus	These pins are bi-directional data bus connecting to the MCU data bus. SPI mode: D0: SCLK D1: SDIN	D[2] : OPEN Other: VDDIO or VSS
CS#	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW in parallel interface.	VDDIO or VSS

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td>R/W# (WR#)</td><td>I</td><td>MPU</td><td rowspan="3"></td><td>This pin is read / write control input pin connecting to the MCU interface.
When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin R/W (WR#) can be connected to either VDDIO or VSS.</td><td>VDDIO or VSS</td></tr>
<tr><td>D/C#</td><td>I</td><td>MPU</td><td>This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the data at D [7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D [7:0] will be interpreted as command.</td><td>VDDIO or VSS</td></tr>
<tr><td>E (RD#)</td><td>I</td><td>MPU</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial interface is selected, this pin E (RD#) should be connected to either VDDIO or VSS</td><td>VDDIO or VSS</td></tr>
<tr><td>RES#</td><td>I</td><td>MPU</td><td>System Reset</td><td>This pin is reset signal input.
Active Low.</td><td>-</td></tr>
<tr><td>BUSY</td><td>O</td><td>MPU</td><td>Device Busy Signal</td><td>This pin is Busy state output pin

When Busy is High, the operation of the chip should not be interrupted, command should not be sent.

e.g., The chip would put Busy pin High when
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor</td><td>Open</td></tr>
<tr><td>CLS</td><td>I</td><td>VDDIO/VSS</td><td>Mode Selection</td><td>This pin is internal clock enable pin.
It should be connected with VDDIO.</td><td>-</td></tr>
<tr><td>CL</td><td>I/O</td><td>NC</td><td>Reserve for Testing</td><td>This pin is Reserved for production testing. Keep it open.</td><td>Open</td></tr>
<tr><td>BS [2:0]</td><td>I</td><td>VDDIO/VSS</td><td>Mode Selection</td><td>These pins are for selecting different bus interface.
BS2 should be connected to VSS.

Table 6-1 : Bus Interface selection
<table>
<tr><td>BS1</td><td>BS0</td><td>MPU Interface</td></tr>
<tr><td>L</td><td>L</td><td>4-lines serial peripheral interface (SPI)</td></tr>
<tr><td>L</td><td>H</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>H</td><td>L</td><td>3-lines serial peripheral interface (SPI) – 9 bits SPI</td></tr>
<tr><td>H</td><td>H</td><td>8-bit 6800 parallel interface</td></tr>
</table></td><td>-</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
TSDA	I/O	Temperature sensor SDA	Interface to Digital Temperature Sensor	This pin is I^2C Interface to digital temperature sensor Data pin External pull up resistor is required when connecting to I^2C slave	Open
TSCL	O	Temperature sensor SCL	Interface to Digital Temperature Sensor	This pin is I^2C Interface to digital temperature sensor Clock pin External pull up resistor is required when connecting to I^2C slave	Open
Analog Pin					
GDR	O	POWER MOSFET Driver Control	PREVGH & PREVGL Generation	This pin is N-Channel MOSFET Gate Drive Control.	-
RESE	I	Booster Control Input		This pin is the Current Sense Input for the Control Loop	-
FB	I	Booster Control Input		This pin is the Feedback Input for the Control Loop	-
PREVGH	C	Stabilizing capacitor		This pin is the Power Supply pin for VGH and VSH. A stabilizing capacitor should be connected between PREVGH and VSS.	-
PREVGL	C	Stabilizing capacitor		This pin is the Power Supply pin for VCOM, VGL and VSL. A stabilizing capacitor should be connected between PREVGL and VSS.	-
VGH	C	Stabilizing capacitor	VGH, VGL Generation	Positive Gate driving voltage. A stabilizing capacitor should be connected between VGH and VSS.	-
VGL	C	Stabilizing capacitor	VGL Generation	This pin is Negative Gate driving voltage. A stabilizing capacitor should be connected between VGL and VSS.	-
VSH	C	Stabilizing capacitor	VSH, VSL Generation	This pin is Positive Source driving voltage. A stabilizing capacitor should be connected between VSH and VSS.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage. A stabilizing capacitor should be connected between VSL and VSS.	-
VCOM	C	Panel/ Stabilizing capacitor	VCOM	This pin is VCOM driving voltage A stabilizing capacitor should be connected between VCOM and VSS.	-
Panel Driving					
S [127:0]	O	Panel	Source driving signal	Source output pin	Open
G [179:0]	O	Panel	Gate driving signal	Gate output pin	Open
VBD	O	Panel	Border driving signal	Border output pin	Open

Pin name	Type	Connect to	Function	Description	When not in use
Others					
NC	NC	NC	Not Connected	Keep open. Do not connect with other NC pins	Open
TPA	NC	NC	Reserve for Testing	Keep open.	Open
TPB	NC	NC	Reserve for Testing	Keep open.	Open
TPC	NC	NC	Reserve for Testing	Keep open.	Open
TPD	NC	NC	Reserve for Testing	Keep open.	Open

7 FUNCTIONAL BLOCK DESCRIPTION

The device can drive an active matrix TFT EPD panel. It composes of 128 source outputs, 180 gate outputs, 1 VBD and 1 VCOM. It contains flexible built-in waveforms to drive the EPD panel.

7.1 MCU Interface

Note
(1) L is connected to V_{SS}
(2) H is connected to V_{DDIO}

7.1.1 MCU Interface selection

SSD1606 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 7-1. Different MCU mode can be set by hardware selection on BS [2:0] pins.

Table 7-1 : MCU interface assignment under different bus interface mode

Pin Name	Data/Command Interface								Control Signal				
Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E (RD#)	R/W# (WR#)	CS#	D/C#	RES#
SPI4	L					NC	SDin	SCLK	L	L	CS#	D/C#	RES#
8-bit 8080	D [7:0]								RD#	WR#	CS#	D/C#	RES#
SPI3	L					NC	SDin	SCLK	L	L	CS#	L	RES#
8-bit 6800	D [7:0]								E	R/W#	CS#	D/C#	RES#

7.1.2 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

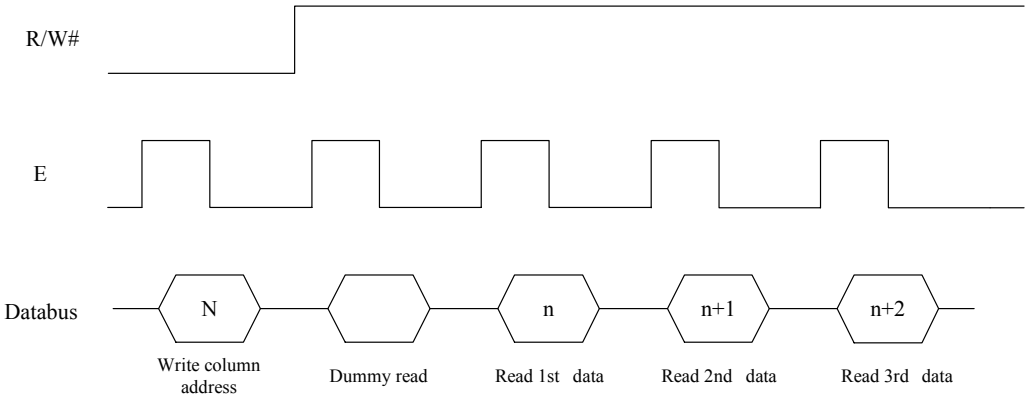
Table 7-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-1.

Figure 7-1 : Data read back procedure - insertion of dummy read



7.1.3 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 7-2 : Example of Write procedure in 8080 parallel interface mode

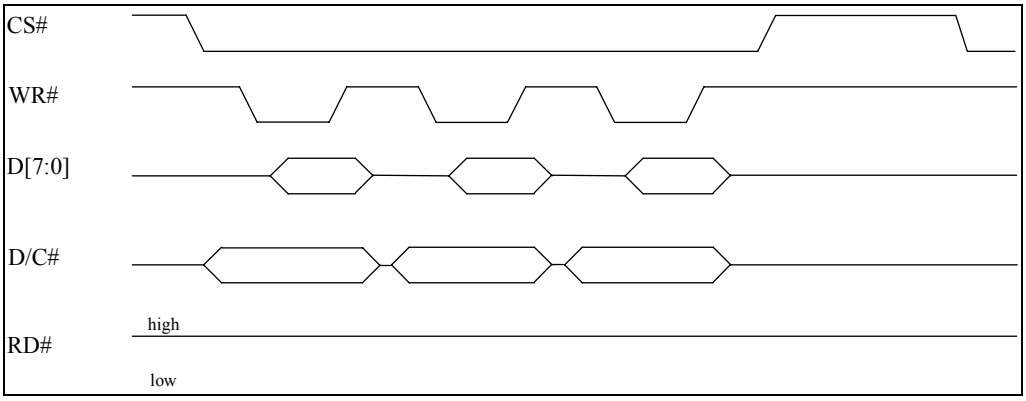


Figure 7-3 : Example of Read procedure in 8080 parallel interface mode

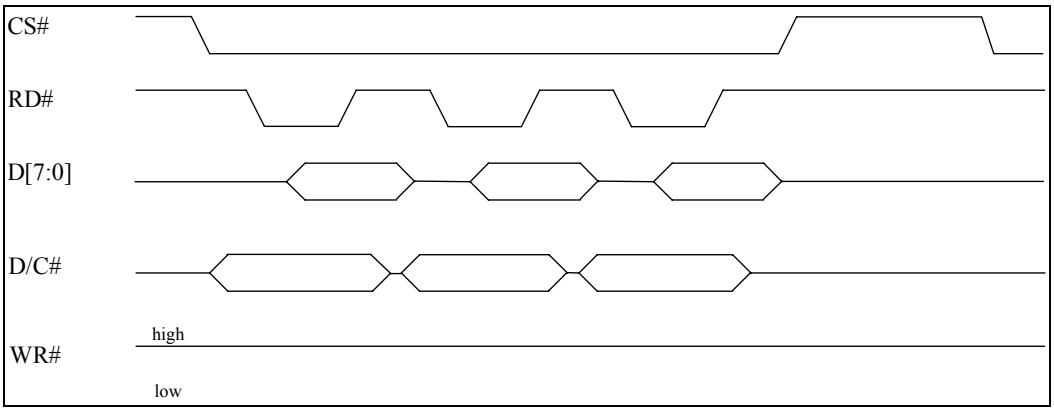


Table 7-3 : Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

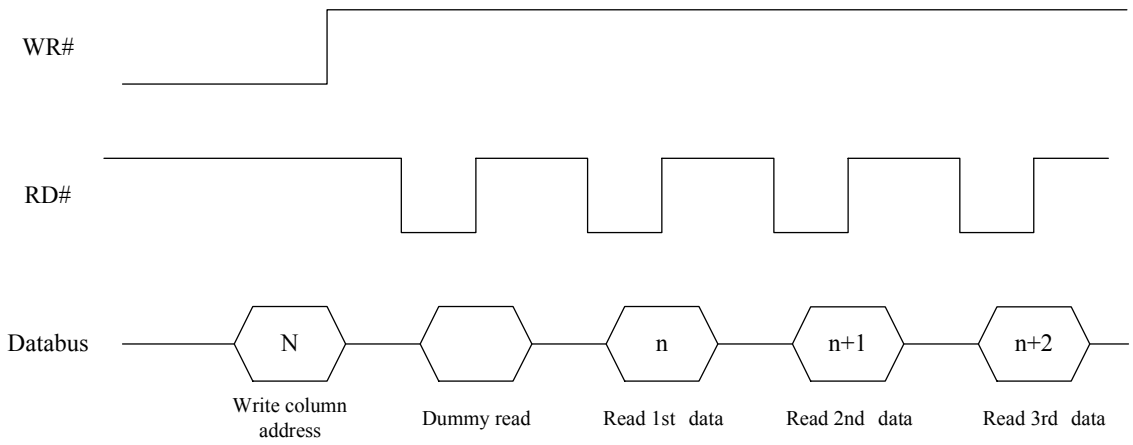
Table 7-4 : Control pins of 8080 interface (Form 2)

Function	RD#	WR#	CS#	D/C#
Write command	H	L	↑	L
Read status	L	H	↑	L
Write data	H	L	↑	H
Read data	L	H	↑	H

Note
(1) ↑ stands for rising edge of signal
(2) Refer to Figure 13-3 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 7-4.

Figure 7-4 : Display data read back procedure - insertion of dummy read



7.1.4 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

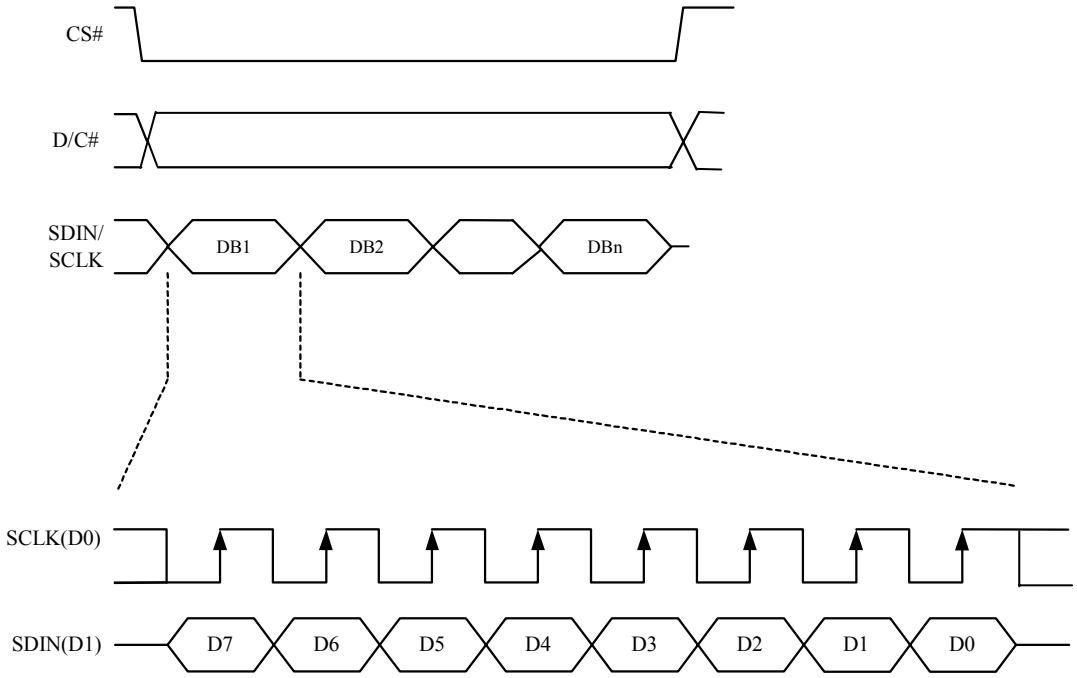
Table 7-5 : Control pins of Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.
Under serial mode, only write operations are allowed.

Figure 7-5 : Write procedure in SPI mode



7.1.5 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#)#, E and D/C# can be connected to an external ground.

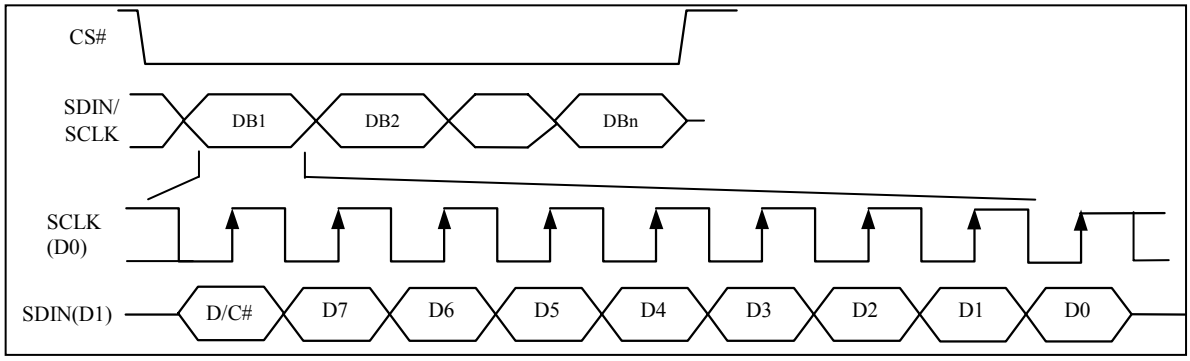
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 7-6 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	SCLK
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) ↑ stands for rising edge of signal

Figure 7-6 : Write procedure in 3-wire Serial interface mode



7.2 RAM

The On chip display RAM is holding the image data. 1 set of RAM is built for historical data and the other set is built for the current image data. The size of each RAM is 128x180x2 bits.

Table 7-7 shows the RAM map under the following condition:

- Command “Data Entry Mode” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to

180 Mux	MUX = B3h
Select G0 as 1st gate	GD = 0
Left and Right gate Interlaced	SM = 0
Scan From G0 to G179	TB = 0

- Command “Gate Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Data byte sequence: DB0, DB1, DB2 … DB5759

Table 7-7 : RAM address map

		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S124	S125	S126	S127	Source X-ADDR
		00h				01h				…		1Fh				
G0	00h	DB0 [7:6]	DB0 [5:4]	DB0 [3:2]	DB0 [1:0]	DB1 [7:6]	DB1 [5:4]	DB1 [3:2]	DB1 [1:0]	…	…	DB31 [7:6]	DB31 [5:4]	DB31 [3:2]	DB31 [1:0]	
G1	01h	DB32 [7:6]	DB32 [5:4]	DB32 [3:2]	DB32 [1:0]	DB33 [7:6]	DB33 [5:4]	DB33 [3:2]	DB33 [1:0]	…	…	DB63 [7:6]	DB63 [5:4]	DB63 [3:2]	DB63 [1:0]	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	
G178	B2h	DB5696 [7:6]	DB5696 [5:4]	DB5696 [3:2]	DB5696 [1:0]	DB5697 [7:6]	DB5697 [5:4]	DB5697 [3:2]	DB5697 [1:0]	…	…	DB5727 [7:6]	DB5727 [5:4]	DB5727 [3:2]	DB5727 [1:0]	
G179	B3h	DB5728 [7:6]	DB5728 [5:4]	DB5728 [3:2]	DB5728 [1:0]	DB5729 [7:6]	DB5729 [5:4]	DB5729 [3:2]	DB5729 [1:0]	…	…	DB5759 [7:6]	DB5759 [5:4]	DB5759 [3:2]	DB5759 [1:0]	
GATE	Y-ADDR															

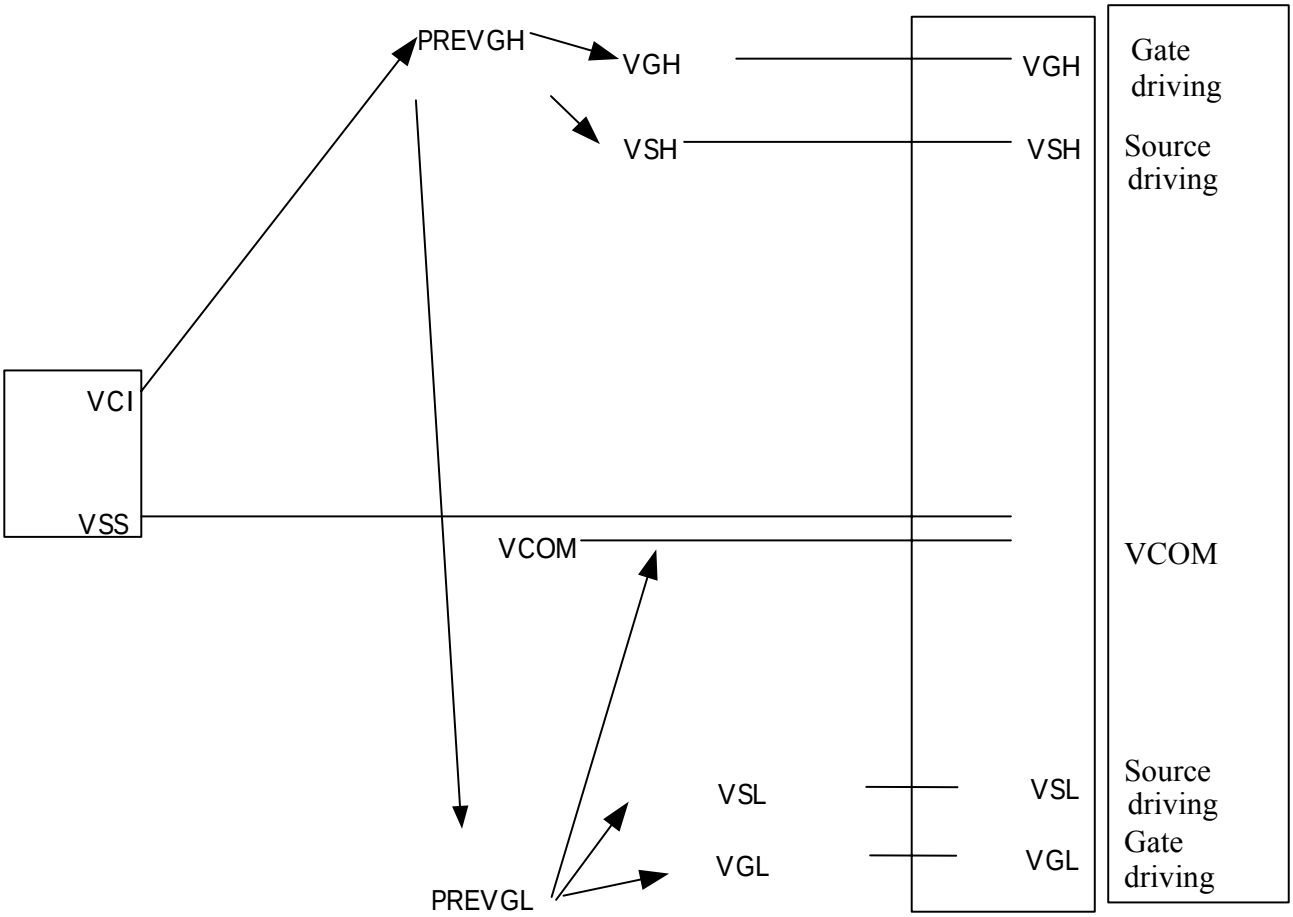
7.3 OSCILLATOR

On-chip oscillator is included for the use on waveform timing and Booster operations.

7.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltage required for an AMEPD panel.

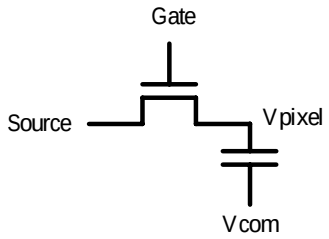
Figure 7-7 : Input and output voltage relation chart



- Max voltage difference between VGH and VGL is 42V.

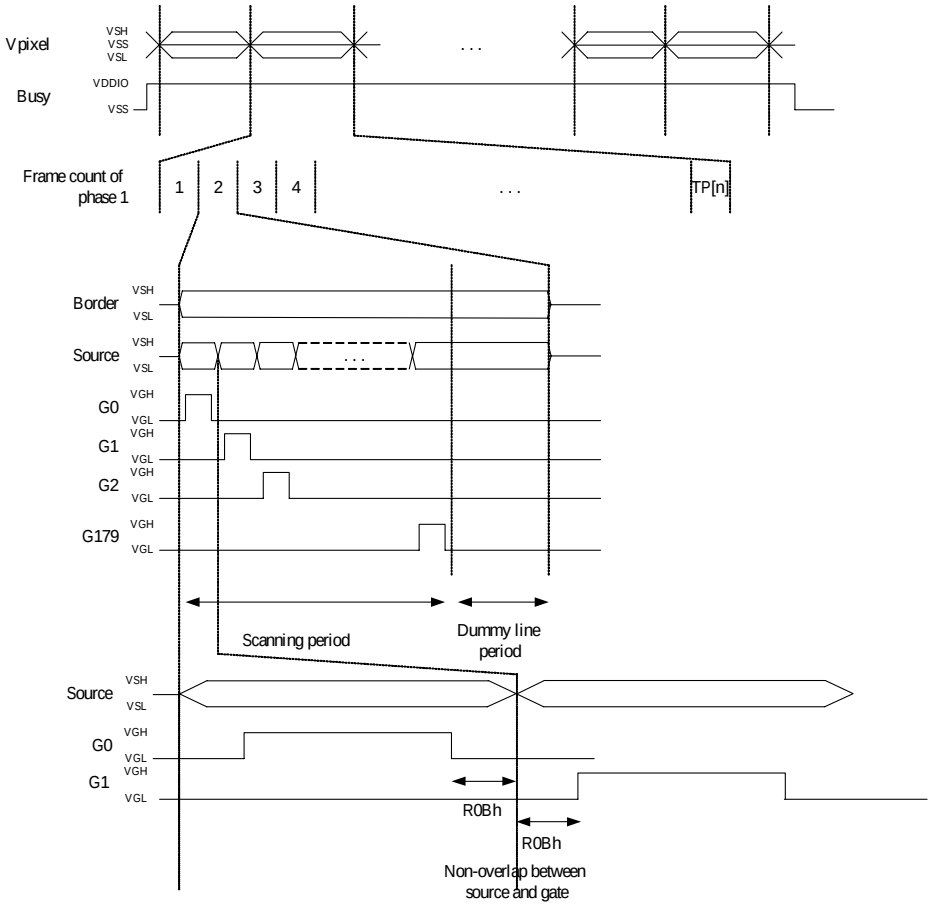
7.5 Panel Driving Waveform

Figure 7-8 : Vpixel Definition



The Vpixel is defined as Figure 7-8, and its relations with GATE, SOURCE are shown below figure.

Figure 7-9 : The Relation of Vpixel Waveform with Gate and Source



7.6 VCOM Functional

7.6.1 VCOM regulation

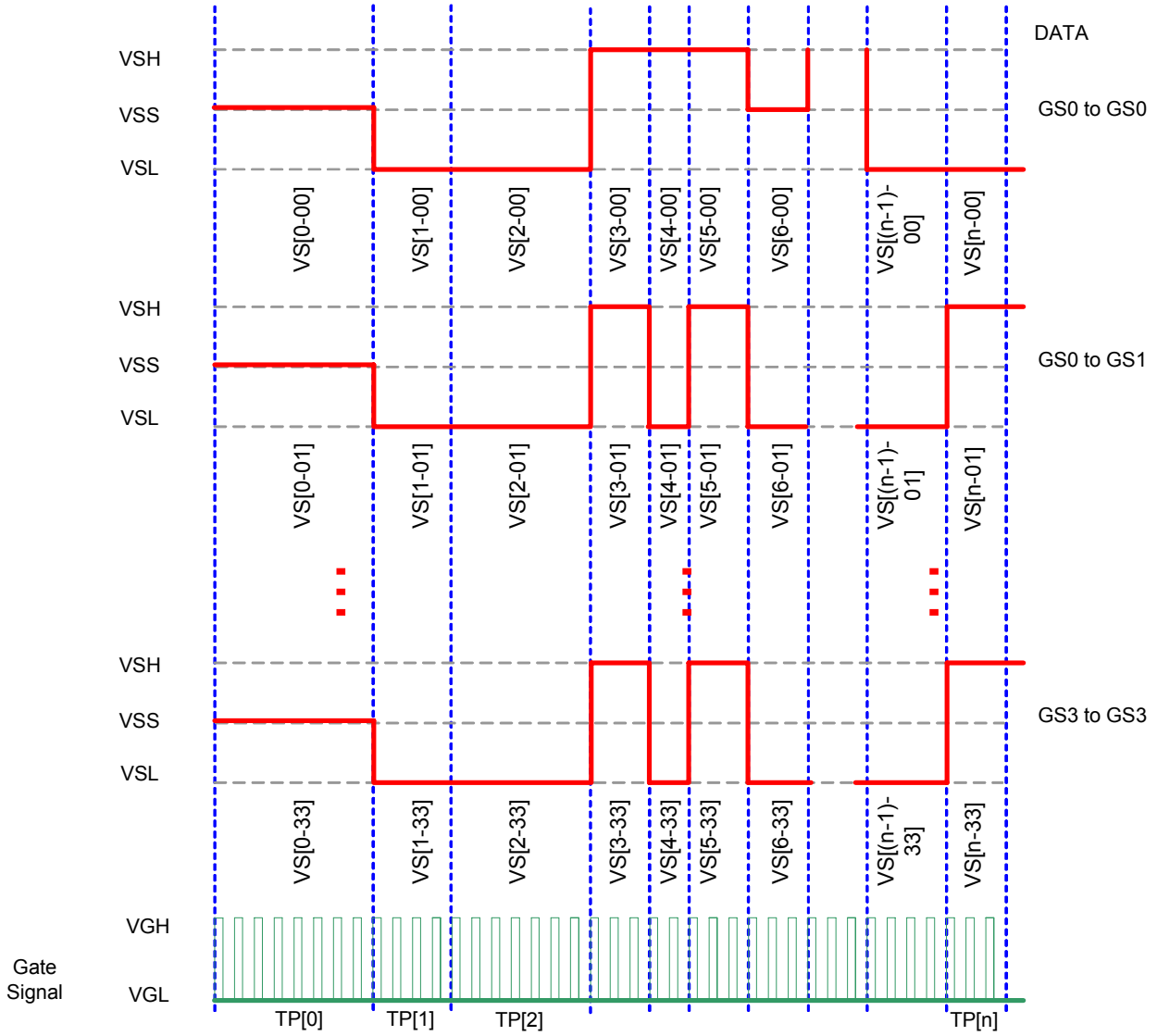
This functional block generates the voltage of VCOM, which are necessary for operating an AMEPD.

7.6.2 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level and programmed the setting into OTP.

7.7 Gate and Programmable Source waveform

Figure 7-10 : Programmable Source and Gate waveform illustration



- There are totally 20 phases for programmable Source waveform of different phase length.
- The phase period defined as TP [n] * T_{FRAME}, where TP [n] range from 0 to 15.
- TP [n] = 0 indicates phase skipped
- Source Voltage Level: VS [n-XY] is constant in each phase
- VS [n-XY] indicates the voltage in phase n for transition from GS X to GS Y
  - 00 – VSS
  - 01 – VSH
  - 10 – VSL
  - 11 – HiZ
- VS [n-XY] and TP[n] are stored in waveform lookup table register [LUT].

7.8 Waveform Look Up Table (LUT)

LUT contains 720bits, which define the display driving waveform settings. They are arranged in following format

Figure 7-11 : VS[n-XY] and TP[n] mapping in LUT

in Decimal	D7	D6	D5	D4	D3	D2	D1	D0
1	VS[0-03]		VS[0-02]		VS[0-01]		VS[0-00]	
2	VS[0-13]		VS[0-12]		VS[0-11]		VS[0-10]	
3	VS[0-23]		VS[0-22]		VS[0-21]		VS[0-20]	
4	VS[0-33]		VS[0-32]		VS[0-31]		VS[0-30]	
5	VS[1-03]		VS[1-02]		VS[1-01]		VS[1-00]	
6	VS[1-13]		VS[1-12]		VS[1-11]		VS[1-10]	
7	VS[1-23]		VS[1-22]		VS[1-21]		VS[1-20]	
8	VS[1-33]		VS[1-32]		VS[1-31]		VS[1-30]	
…	…		…		…		…	
77	VS[19-03]		VS[19-02]		VS[19-01]		VS[19-00]	
78	VS[19-13]		VS[19-12]		VS[19-11]		VS[19-10]	
79	VS[19-23]		VS[19-22]		VS[19-21]		VS[19-20]	
80	VS[19-33]		VS[19-32]		VS[19-31]		VS[19-30]	
81	TP[1]				TP[0]			
82	TP[3]				TP[2]			
…	…				…			
90	TP[19]				TP[18]			

7.9 OTP

The OTP is the non-volatile memory and stored the information of:

- OTP Selection Option
- VCOM value
- 11 set of WAVEFORM SETTING (WS) [720bits x 11]
- 10 set of TEMPERATURE RANGE (TR) [24bits x 10]

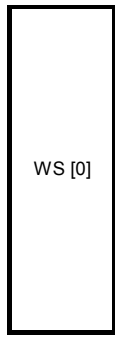
For Programming the WS and TR, Write RAM is required, and the configurations should be

Command: Data Entry mode	C11, D03	Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction
Command: X RAM address start /end	C44, D00, D1F	Set RAM Address for S0 to S127
Command: Y RAM address start /end	C45, D00, DB3	Set RAM Address for G0 to G179
Command: RAM X address counter	C4E, D00	Set RAM X AC as 0
Command: RAM Y address counter	C4F, D00	Set RAM Y AC as 0

The mapping table of OTP is shown in below figure,

Figure 7-12 : OTP Content and Address Mapping

WRITE RAM ADDRESS		D7	D6	D5	D4	D3	D2	D1	D0
X	Y								
NA	NA	VCOM							
0	0	VS[0-03]		VS[0-02]		VS[0-01]		VS[0-00]	
1	0	VS[0-13]		VS[0-12]		VS[0-11]		VS[0-10]	
2	0	VS[0-23]		VS[0-22]		VS[0-21]		VS[0-20]	
3	0	VS[0-33]		VS[0-32]		VS[0-31]		VS[0-30]	
4	0	VS[1-03]		VS[1-02]		VS[1-01]		VS[1-00]	
…	…	…		…		…		…	
14	2	VS[19-23]		VS[19-22]		VS[19-21]		VS[19-20]	
15	2	VS[19-33]		VS[19-32]		VS[19-31]		VS[19-30]	
16	2	TP[1]				TP[0]			
17	2	TP[3]				TP[2]			
…	…	…				…			
25	2	TP[19]				TP[18]			
26	2	WS[1]							
…	…								
19	5								
…	…	…							
…	…								
4	28	WS[10]							
…	…								
29	30								
30	30	TEMP[1-L][7:0]							
31	30	TEMP[1-H][3:0]				TEMP[1-L][11:8]			
0	31	TEMP[1-H][11:4]							
1	31	TEMP[2-L][11:0]							
2	31								
3	31	TEMP[2-H][11:0]							
…	…	…							
…	…								
22	31	TEMP[9-L][11:0]							
23	31								
24	31	TEMP[9-H][11:0]							
25	31	TEMP[10-L][11:0]							
26	31								
27	31	TEMP[10-H][11:0]							



Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

7.10 Temperature Searching Mechanism

Legend:

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	720 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing reading from temperature sensor (volatile)
OTP	A non-volatile storing 11 sets of waveform setting and 10 set of temperature range
WS_sel_address	an address pointer indicating the selected WS#

Figure 7-13 : Waveform Setting and Temperature Range # mapping

OTP (non-volatile)

WS0	
WS1	TR1
WS2	TR2
WS3	TR3
WS4	TR4
WS5	TR5
WS6	TR6
WS7	TR7
WS8	TR8
WS9	TR9
WS10	TR10

IC implementation requirement	
1	Default selection is **WS0**
2	Compare temperature register from **TR1 to TR10**, in sequence. **The last match will be recorded**
	i.e. If the temperature register fall in both TR5 and TR7. WS7 will be selected
3	If none of the range TR1 to TR10 is match, WS0 will be selected.
User application	
1	The default waveform should be programmed as WS0
2	There is no restriction on the sequence of TR1, TR2…. TR10.

7.11 External Temperature Sensor I2C Single Master Interface

The chip provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing.
TSDA will treat as SDA line and TSCL will treat as SCL line. They are required connecting with external pull-up resistor.

1. If the Temperature value MSByte bit D11 = 0, then
The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

8 COMMAND TABLE

Table 8-1: Command Table

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
1	0	-	0	0	0	0	0	A_2	A_1	A_0	Status Read	Read Driver status on • A2: BUSY flag • A1,A0: Chip ID (01 as default)
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[7:0]: MUX setting as A[7:0] + 1 POR = B3h + 1 MUX B[2:0]: Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD='0', G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … [POR] GD='1', G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0, G0, G1, G2, G3…G179 (left and right gate interlaced) [POR] SM=1, G0, G2, G4 …G178, G1, G3, …G179 B[0]: TB TB = 0, scan from G0 to G179 [POR] TB = 1, scan from G179 to G0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	02	0	0	0	0	0	0	1	0	Reserve	
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[7:4]: VGH, 15 to 22V in 0.5V step
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
												VGH 0000 15.0 0001 15.5 0010 16.0 0011 16.5 0100 17.0 0101 17.5 0110 18.0 0111 18.5 1000 19.0 1001 19.5 1010 20.0 1011 20.5 1100 21.0 1101 21.5 1110 22.0 [POR] Others N/A A[3:0]: VGL, -15 to -20V in 0.5V step VGL default at -20V VGL 0000 -15.0 0001 -15.5 0010 -16.0 0011 -16.5 0100 -17.0 0101 -17.5 0110 -18.0 0111 -18.5 1000 -19.0 1001 -19.5 1010 -20.0 [POR] Others N/A
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude A[3:0]: VSH/VSL 10V to 17V in 0.5V step VSH/VSL 0000 10.0 0001 10.5 0010 11.0 0011 11.5 0100 12.0 0101 12.5 0110 13.0 0111 13.5 1000 14.0 1001 14.5 1010 15.0 [POR] 1011 15.5 1100 16.0 1101 16.5 1110 17.0 Others N/A
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	05	0	0	0	0	0	1	0	1	Reserve	

Fundamental Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>06</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Display Control</td><td rowspan="2">Display control setting
A[0]: Grey Scale (GS) mode (1bit)
Mono vs 4 GS
A[0] = 0: 4GS [POR]
A[0] = 1: Mono

In mono mode,
Data 00, 01 will be treat as 0,
Data 10,11 will be treat as 1
Only use transition between
GS0 to GS0 or GS3
GS3 to GS0 or GS3

<table><tr><th>A[4]</th><th>A[5]</th><th>Description</th></tr><tr><td>1</td><td>1</td><td>All Gate output voltage level as VGH</td></tr><tr><td>1</td><td>0</td><td>All Gate output voltage level as VGL</td></tr><tr><td>0</td><td>1</td><td>Selected gate output as VGL, non-selected gate output as VGH</td></tr><tr><td>0</td><td>0</td><td>Selected gate output as VGH, non-selected gate output as VGL
[POR]</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>0</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>08</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>09</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0A</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0B</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Gate and Source non overlap period Control</td><td rowspan="2">Set Delay of gate and source non overlap period
Gate falling edge to source output change
Source change to Gate rising edge

Delay Duration in terms of Oscillator clock [$1/F_{OSC}$]
<table><tr><th>A [3:0]</th><th>Delay Duration</th></tr><tr><td>0000</td><td>0</td></tr><tr><td>0001</td><td>2</td></tr><tr><td>0010</td><td>4</td></tr><tr><td>…</td><td></td></tr><tr><td></td><td></td></tr><tr><td>0101</td><td>10 [POR]</td></tr><tr><td>…</td><td></td></tr><tr><td>1110</td><td>28</td></tr><tr><td>1111</td><td>30</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>0C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0D</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0E</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0F</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Gate scan start</td><td>Set the scanning start position of the</td></tr>
</table>

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	position	gate driver. The valid range is from 0 to 179. TB=0: SCN [7:0] = A[7:0] 00h [POR] TB=1: SCN [7:0] = 179 - A[7:0] 00h [POR]
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A_0		A[0] : Description 0 [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0]: Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2]: Set the direction in which the address counter is updated automatically after data are written to the RAM. A[2] = 0, the address counter is updated in the X direction. [POR] A[2] = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command
0	0	13	0	0	0	1	0	0	1	1	Reserve	
0	0	14	0	0	0	1	0	1	0	0	Reserve	
0	0	15	0	0	0	1	0	1	0	1	Reserve	
0	0	16	0	0	0	1	0	1	1	0	Reserve	
0	0	17	0	0	0	1	0	1	1	1	Reserve	
0	0	18	0	0	0	1	1	0	0	0	Reserve	
0	0	19	0	0	0	1	1	0	0	1	Reserve	
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	1B	0	0	0	1	1	1	0	1	Temperature Sensor Control (Read from	Read from temperature register. X[7:0] – MSByte
1	1		X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0		

Fundamental Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
1	1		Y_7	Y_6	Y_5	Y_4	0	0	0	0	temperature register)	Y[7:4] – LSByte
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to temperature sensor)	Write Command to temperature sensor A[7:6] – Select no of byte to be sent 00 – Address + pointer 01 – Address + pointer + 1st parameter 10 – Address + pointer + 1st parameter + 2nd pointer 11 – Address A[5:0] – Pointer Setting B[7:0] – 1st parameter C[7:0] – 2nd parameter The command required CLKEN=1.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	1D	0	0	0	1	1	1	0	1	Temperature Sensor Control (Load temperature register with temperature sensor reading)	Load temperature register with temperature sensor reading BUSY=H for whole loading period The command required CLKEN=1.
0	0	1E	0	0	0	1	1	1	1	0	Reserve	
0	0	1F	0	0	0	1	1	1	1	1	Reserve	
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update	Option for Display Update

<table>
<tr><th colspan="12">Fundamental Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Control 1</td><td>Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A [7]
1 Enable bypass
0 Disable bypass [POR]

A[5:4] value will be used as for bypass
00 [POR]

A[3:0] Initial Update Option - Source Control

<table><tr><th></th><th>GSC A[3:2]</th><th>GSD A[1:0]</th></tr><tr><td>0000</td><td>GS0</td><td>GS0</td></tr><tr><td>0001</td><td>GS0</td><td>GS1</td></tr><tr><td>0010</td><td>GS0</td><td>GS2</td></tr><tr><td>0011 [POR]</td><td>GS0</td><td>GS3</td></tr><tr><td>0100</td><td>GS1</td><td>GS0</td></tr><tr><td>0101</td><td>GS1</td><td>GS1</td></tr><tr><td>0110</td><td>GS1</td><td>GS2</td></tr><tr><td>0111</td><td>GS1</td><td>GS3</td></tr><tr><td>1000</td><td>GS2</td><td>GS0</td></tr><tr><td>1001</td><td>GS2</td><td>GS1</td></tr><tr><td>1010</td><td>GS2</td><td>GS2</td></tr><tr><td>1011</td><td>GS2</td><td>GS3</td></tr><tr><td>1100</td><td>GS3</td><td>GS0</td></tr><tr><td>1101</td><td>GS3</td><td>GS1</td></tr><tr><td>1110</td><td>GS3</td><td>GS2</td></tr><tr><td>1111</td><td>GS3</td><td>GS3</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update</td><td>Display Update Sequence Option:</td></tr>
</table>

Fundamental Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Control 2</td><td>Enable the stage for Master Activation

<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF
[POR]</td></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature value
Then Load LUT
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>F7</td></tr><tr><td>To Enable Clock Signal
(CLKEN=1)</td><td>80</td></tr><tr><td>To Enable Clock Signal,
then Enable CP
(CLKEN=1, CPEN=1)</td><td>C0</td></tr><tr><td>To INITIAL DISPLAY + PATTEN DISPLAY</td><td>0C</td></tr><tr><td>To INITIAL DISPLAY</td><td>08</td></tr><tr><td>To DISPLAY PATTEN</td><td>04</td></tr><tr><td>To Disable CP,
then Disable Clock Signal
(CLKEN=1, CPEN=1)</td><td>03</td></tr><tr><td>To Disable Clock Signal
(CLKEN=1)</td><td>01</td></tr></table>
Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC
If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC
AND
INTERNAL CLOCK Signal = VSS,</td></tr>
<tr><td>0</td><td>0</td><td>23</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>25</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Read RAM</td><td>After this command, data read on the MCU bus will fetch data from RAM, until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserve</td><td></td></tr>
</table>

Fundamental Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds 0x09(10Seconds) [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2B	0	0	1	0	1	0	1	1	Reserve	
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM register	Write VCOM register from MCU interface
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	2D	0	0	1	0	1	1	0	1	Read OTP Registers	Read register reading to MCU A [7:0] Spare OTP Option B [7:0] VCOM Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	2E	0	0	1	0	1	1	1	0	Reserve	
0	0	2F	0	0	1	0	1	1	1	1	Reserve	
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	31	0	0	1	1	0	0	0	1	Reserve	
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU [720 bits]
0 0 0 … 0 0	1 1 1 … 1 1		LUT [90 bytes]									
0	0	33	0	0	1	1	0	0	1	1	Read LUT register	Read from LUT register (excluding temperature data) [720 bits]
1 1 1 … 1 1	1 1 1 … 1 1		LUT [90 bytes]									
0	0	34	0	0	1	1	0	1	0	0	Reserve	
0	0	35	0	0	1	1	0	1	0	1	Reserve	
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R36h]
0	0	37	0	0	1	1	0	1	1	1	OTP selection	Write the OTP Selection:

<table>
<tr><th colspan="12">Fundamental Command Table</th></tr>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Control</td><td><table><tr><td>A[7]=1</td><td>spare VCOM OTP</td></tr><tr><td>A[6]</td><td>VCOM_Status</td></tr><tr><td>A[5]=1</td><td>spare WS OTP</td></tr><tr><td>A[4]</td><td>WS_Status</td></tr></table>
A3:A0 are reserved OTP bit. User can treat the bits as Version Control.</td></tr>
<tr><td>0</td><td>0</td><td>38</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Reserve</td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Set dummy line period</td><td rowspan="2">Set number of dummy line period

A[6:0]: Number of dummy line period in term of TGate
4 [POR]
Available setting 0 to 127.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Set Gate line width</td><td rowspan="2">Set Gate line width (TGate)
A[3:0] Line width in us

<table><tr><td>0000</td><td>60</td></tr><tr><td>0001</td><td>64</td></tr><tr><td>0010</td><td>68</td></tr><tr><td>0011</td><td>72</td></tr><tr><td>0100</td><td>78</td></tr><tr><td>0101</td><td>84</td></tr><tr><td>0110</td><td>90</td></tr><tr><td>0111</td><td>98</td></tr><tr><td>1000</td><td>108 [POR]</td></tr><tr><td>1001</td><td>120</td></tr><tr><td>1010</td><td>136</td></tr><tr><td>1011</td><td>154</td></tr><tr><td>1100</td><td>180</td></tr><tr><td>1101</td><td>216</td></tr><tr><td>1110</td><td>272</td></tr><tr><td>1111</td><td>362</td></tr></table>
Remark: Default value will give 50Hz Frame frequency under 4 dummy line pulse setting.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Border Waveform</td><td>Select border waveform for VBD</td></tr>
</table>

Fundamental Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Control	A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD 00 VSS 01 VSH 10 VSL 11[POR] HiZ A [3:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) 0000 GS0 GS0 0001 GS0 GS1 0010 GS0 GS2 0011 [POR] GS0 GS3 0100 GS1 GS0 0101 GS1 GS1 0110 GS1 GS2 0111 GS1 GS3 1000 GS2 GS0 1001 GS2 GS1 1010 GS2 GS2 1011 GS2 GS3 1100 GS3 GS0 1101 GS3 GS1 1110 GS3 GS2 1111 GS3 GS3
0	0	3D	0	0	1	1	1	1	0	1	Reserve	
0	0	3E	0	0	1	1	1	1	1	0	Reserve	
0	0	3F	0	0	1	1	1	1	1	1	Reserve	
0	0	40	0	1	0	0	0	0	0	0	Reserve	
0	0	41	0	1	0	0	0	0	0	1	Reserve	
0	0	42	0	1	0	0	0	0	1	0	Reserve	
0	0	43	0	1	0	0	0	0	1	1	Reserve	
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		address unit A[7:0]: XStart, POR = 00h B[7:0]: XEnd, POR = 1Fh
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: YStart, POR = 00h B[7:0]: YEnd, POR = B3h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	46	0	1	0	0	0	1	1	0	Reserve	
0	0	47	0	1	0	0	0	1	1	1	Reserve	
0	0	48	0	1	0	0	1	0	0	0	Reserve	
0	0	49	0	1	0	0	1	0	0	1	Reserve	
0	0	4A	0	1	0	0	1	0	1	0	Reserve	
0	0	4B	0	1	0	0	1	0	1	1	Reserve	
0	0	4C	0	1	0	0	1	1	0	0	Reserve	
0	0	4D	0	1	0	0	1	1	0	1	Reserve	
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) POR is 0
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) POR is 0
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	F0	1	1	1	1	0	0	0	0	Booster Feedback Selection	Set Booster Feedback selection 0x1F = Internal Feedback is used POR is 0x1F
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

9 Command DESCRIPTION

9.1 Fundamental command description

9.1.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
POR		1	0	1	1	0	0	1	1
W	1						GD	SM	TB
POR							0	0	0

MUX[7:0]: Specify number of lines for the driver: MUX[7:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 180MUX.

GD: Selects the 1st output Gate

This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM: Change scanning order of gate driver.

When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 180 MUX ratio):

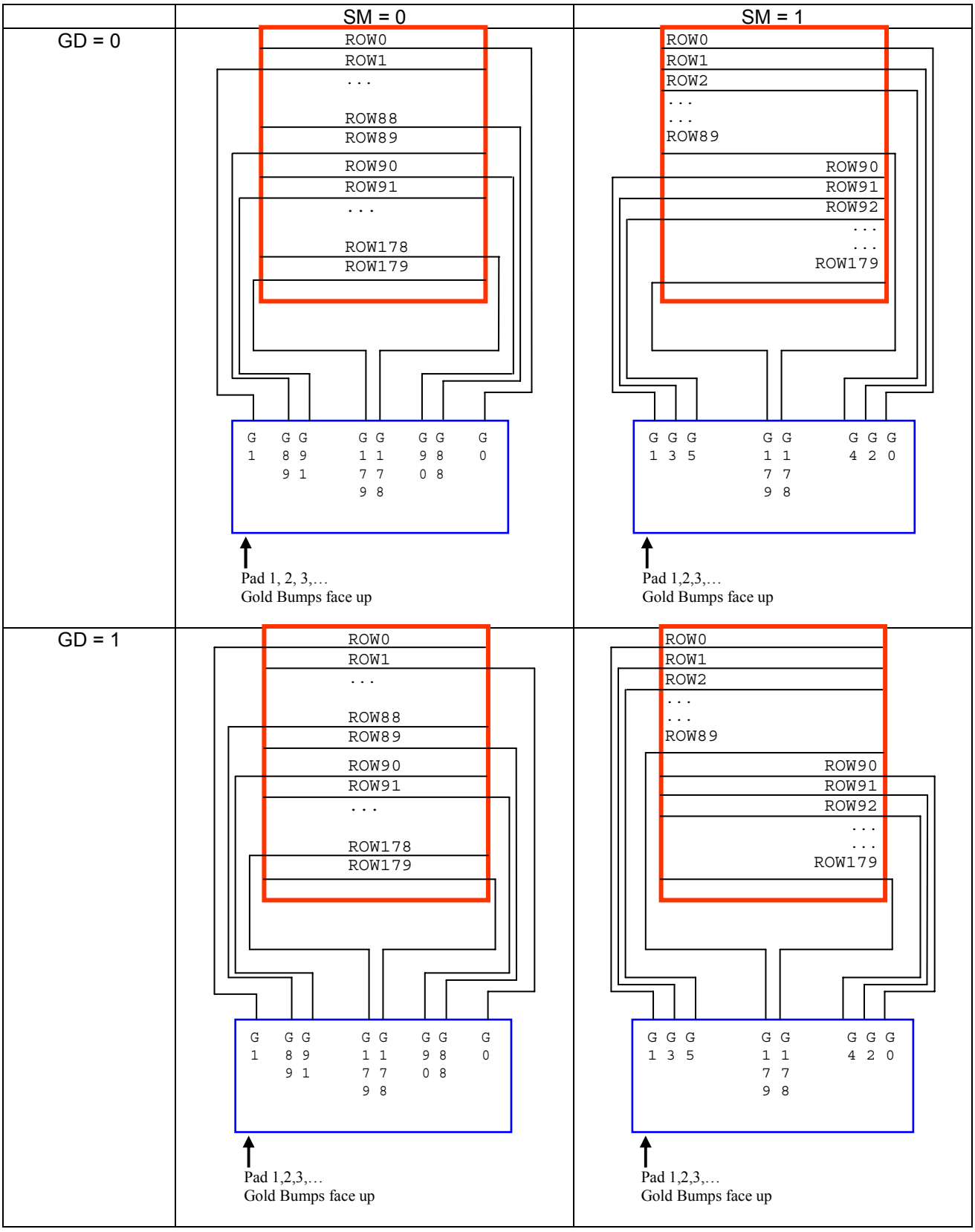
	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW90
G1	ROW1	ROW0	ROW90	ROW0
G2	ROW2	ROW3	ROW1	ROW91
G3	ROW3	ROW2	ROW91	ROW1
:	:	:	:	:
G88	ROW88	ROW89	ROW44	ROW134
G89	ROW89	ROW88	ROW134	ROW44
G90	ROW90	ROW91	ROW45	ROW135
G91	ROW91	ROW90	ROW135	ROW45
:	:	:	:	:
G176	ROW176	ROW177	ROW88	ROW178
G177	ROW177	ROW176	ROW178	ROW88
G178	ROW178	ROW179	ROW89	ROW179
G179	ROW179	ROW178	ROW179	ROW89

See “Scan Mode Setting” on next page.

TB: Change scanning direction of gate driver.

This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

Figure 9-1: Output pin assignment on different Scan Mode Setting



9.1.2 Gate Scan Start Position (0Fh)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 179. Figure 9-2 shows an example using this command of this command when MUX ratio= 180 and MUX ratio= 90 “ROW” means the graphic display data RAM row.

Figure 9-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = 179	MUX ratio (01h) = 89	MUX ratio (01h) = 89
GATE Pin	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 0	Gate Start Position (0Fh) = 45
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G43	:	:	-
G44	:	:	-
G45	:	:	ROW45
G46	:	:	ROW46
:	:	:	:
:	:	:	:
G88	ROW88	ROW88	:
G89	ROW89	ROW89	:
G90	ROW90	-	:
G91	ROW91	-	:
:	:	:	:
	:	:	:
G133	:	:	ROW133
G134	:	:	ROW134
G135	:	:	-
G136	:	:	-
	:	:	:
:	:	:	:
G176	ROW176	-	-
G177	ROW177	-	-
G178	ROW178	-	-
G179	ROW179	-	-
Display Example			

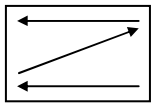
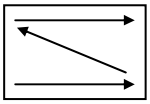
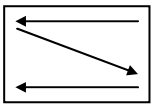
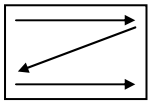
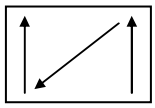
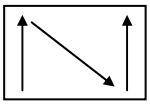
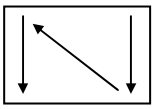
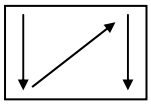
9.1.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

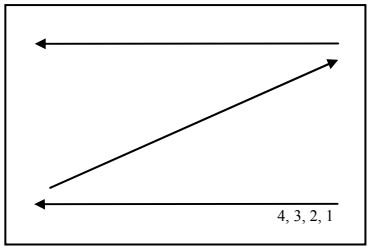
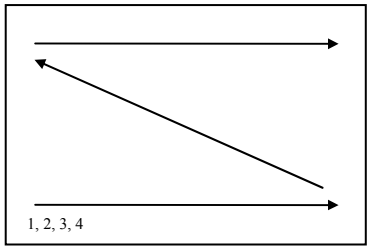
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	0	0

ID[1:0]: The address counter is automatically incremented by 1, after data are written to the RAM when ID[1:0] = “1”. The address counter is automatically decremented by 1, after data are written to the RAM when ID[1:0] = “0”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the RAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]="01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  1F,B3h	00,00h  1F,B3h	00,00h  1F,B3h	00,00h  1F,B3h
AM="1” Y-mode	00,00h  1F,B3h	00,00h  1F,B3h	00,00h  1F,B3h	00,00h  1F,B3h

The pixel sequence are defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X	00,00h  4, 3, 2, 1 1F,B3h	00,00h  1, 2, 3, 4 1F,B3h

9.1.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	1	1	1	1

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 4 times address unit. Data are written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 1Fh. The windows is followed by the control setting of Data Entry Setting (R11h)

9.1.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR		0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	1	0	1	0	0	1	1

YSA[7:0]/YEA[7:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data are written to the RAM within the area determined by the addresses specified by YSA [7:0] and YEA [7:0]. These addresses must be set before the RAM write.
It allows YEA [7:0] ≤ YSA [7:0]. The settings follow the condition on 00h ≤ YSA [7:0], YEA [7:0] ≤ B3h. The windows is followed by the control setting of Data Entry Setting (R11h)

9.1.6 Reserve (46-4Dh)

9.1.7 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[7:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new RAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AD, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

10 Typical Operating Sequence

10.1 Normal Display

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	
2	User	-	HW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Select Border waveform	
4		-	Data operations	
	User	C 11	Command: Data Entry mode	
	User	C 44	Command: X RAM address start /end	
	User	C 45	Command: Y RAM address start /end	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write display data to RAM	
			Ram Content for Display	
5	User	C F0 D 1F	Command: Set Internal Feedback Selection	
6	User	C 20	Command: Display update	
	IC	-	Booster and regulators turn on	
	IC	-	Load temperature register with sensor reading	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
6	User	-	IC power off;	

OTP Selection bit:

Set on R37h, and read from R2Dh, A[7:6] used for VCOM and A[5:4] used for OTP

A[7:6] / [5:4]	Description
00	It indicates fresh device, OTP read and program would be made on Default OTP set User required setting and programming the bits into 01.
01	It indicates default OTP programmed device, OTP read would be made on Default OTP set. User require setting and programming the bits into 11
11	It indicates SPARE OTP programmed device, only OTP read would be made on SPARE

	OTP set. User should stop the OTP programming if 11 is found at OTP checking stage

10.2 VCOM OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
3	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
4	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
5	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait until BUSY = L	
6	User	C 36	Program OTP selection register	
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
7		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 01	Command: Panel configuration (MUX, Source gate scanning direction)	
	User	C 03	Command: VGH, VGL voltage	
	User	C 04	Command: VSH / VSL voltage	
	User	C 3A	Command: Set dummy line pulse period	
	User	C F0 D 1F	Command: Set Internal Feedback Selection	
	User	C 32	VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 22 D 40 C 20	Command: Booster on and High voltage ready	
	User	-	Wait until BUSY = L	
8	User	C 28	Command: Enter VCOM sensing mode	
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	Wait for 10s	According to R29h
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	
9	User	C 22 D 02 C 20	Command: Booster and High voltage disable	
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: VCOM OTP program	
	User	-	Wait until BUSY = L	
11	User	C 22	Command: CLKEN=0	

		D 01 C 20		
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

10.3 WS OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
4	User	C 2D	Check whether the IC status and determine whether "default" or "spare" OTP should be used	
5	User		If the IC had been OTP twice (both default and spare had been used up). The operation should stop	
6	User	C 37	Proceed OTP sequence. Command: Indicate which OTP location to be use (default or spare)	OTP selection register
	User	C 22 D 80 C 20	Command: CLKEN=1	
	User	-	Wait BUSY = L	
7	User	C 36	Program OTP selection register	
	User	-	Wait BUSY = L	
8	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT (11 entries + Temperature range) must be written at the same time	
	User	C 4E D 00 C 4F D 00	Command: Initial Ram address counter	
9	User	C 30	Waveform Setting OTP programming	
	IC	-	BUSY pin pull H	
	IC	-	Check the OTP Selection	
	IC	-	IC control OTP programming time, and transfer data to selected OTP	
	IC	-	BUSY pin pull L	
	User	-	Wait BUSY = L	
10	User	C 22 D 01 C 20	Command: CLKEN=0	
	User	-	Wait BUSY = L	
11	User	-	IC power off	

11 ABSOLUTE MAXIMUM RATING

Table 11-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +3.6	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. This device is not radiation protected.

12 ELECTRICAL CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 12-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{CI}	VCI operation voltage		VCI	2.4	3.0	3.3	V
V_{DD}	VDD operation voltage		VDD	1.7	1.8	1.9	V
V_{COM}	VCOM output voltage		VCOM	-4.0		-0.2	V
V_{GATE}	Gate output voltage		G0-179	-20		+22	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage		G0-179			42	V
V_{SH}	Positive Source output voltage		S0-127	+10		+17	V
V_{SL}	Negative Source output voltage		S0-127		-VSH		V
V_{IH}	High level input voltage			$0.8V_{DDIO}$			V
V_{IL}	Low level input voltage					$0.2V_{DDIO}$	V
V_{OH}	High level output voltage	IOH = -100uA		$0.9V_{DDIO}$			V
V_{OL}	Low level output voltage	IOL = 100uA				$0.1V_{DDIO}$	V
V_{PP}	OTP Program voltage		VPP		7.5		V

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Idslp_VCI	Deep Sleep mode current	VCI=3.3V DC/DC OFF No clock No output load Ram data not retain	V_{CI}		2	5	uA
Islp_VCI	Sleep mode current	VCI=3.3V DC/DC OFF No clock No output load Ram data retain	VCI		35	50	uA
Iopr_VCI	Operating current	VCI=3.3V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. No RAM read/write No OTP read /write Osc on Bandgap on	VCI		2000		uA
V_{GH}	Operating Mode Output Voltage	VCI=3.3V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. Osc on Bandgap on	VGH	21	22	23	V
V_{SH}			VSH	14.5	15	15.5	V
V_{COM}			VCOM	-2.5	-2	-1.5	V
V_{SL}			VSL	-15.5	-15	-14.5	V
V_{GL}			VGL	-21	-20	-19	V

Table 12-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 22V	VGH			400	uA
IVGL	VGL current	VGL = -20V	VGL			600	uA
IVSH	VSH current	VSH = +15V	VSH			4000	uA
IVSL	VSL current	VSL = -15V	VSL			4000	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

13 AC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 13-1: AC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.3V	CL	0.95	1	1.05	MHz

13.1 Interface Timing

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.3V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 13-1 : 6800-series MCU parallel interface characteristics

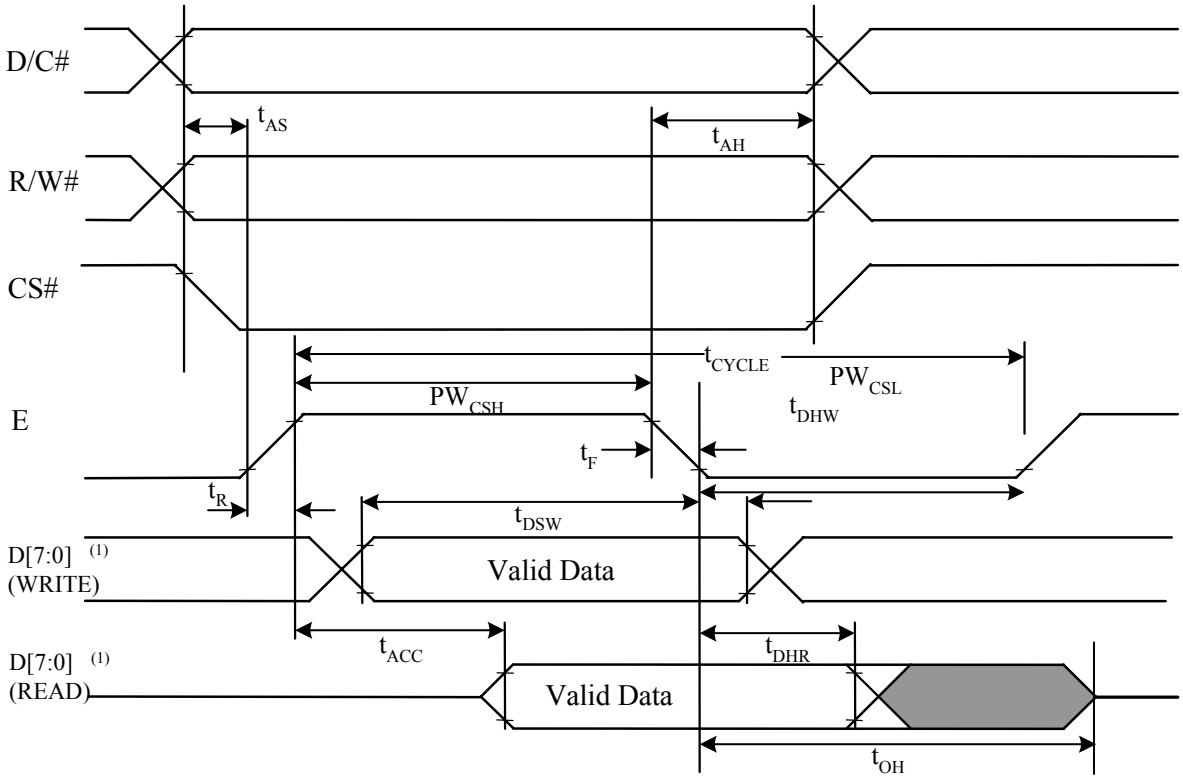


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.3V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 13-2 : 8080-series parallel interface characteristics (Form 1)

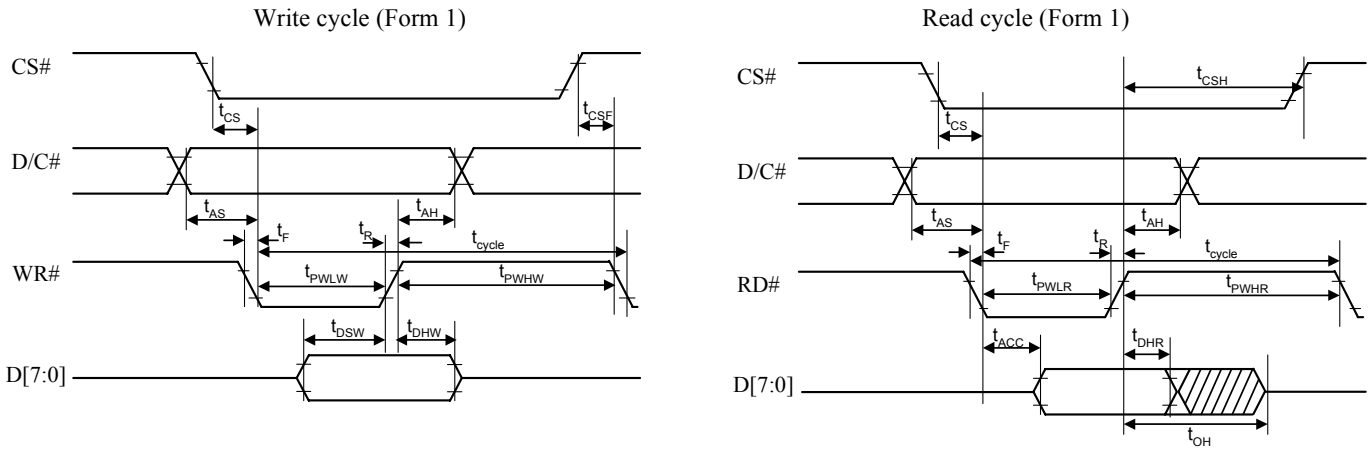


Figure 13-3 : 8080-series parallel interface characteristics (Form 2)

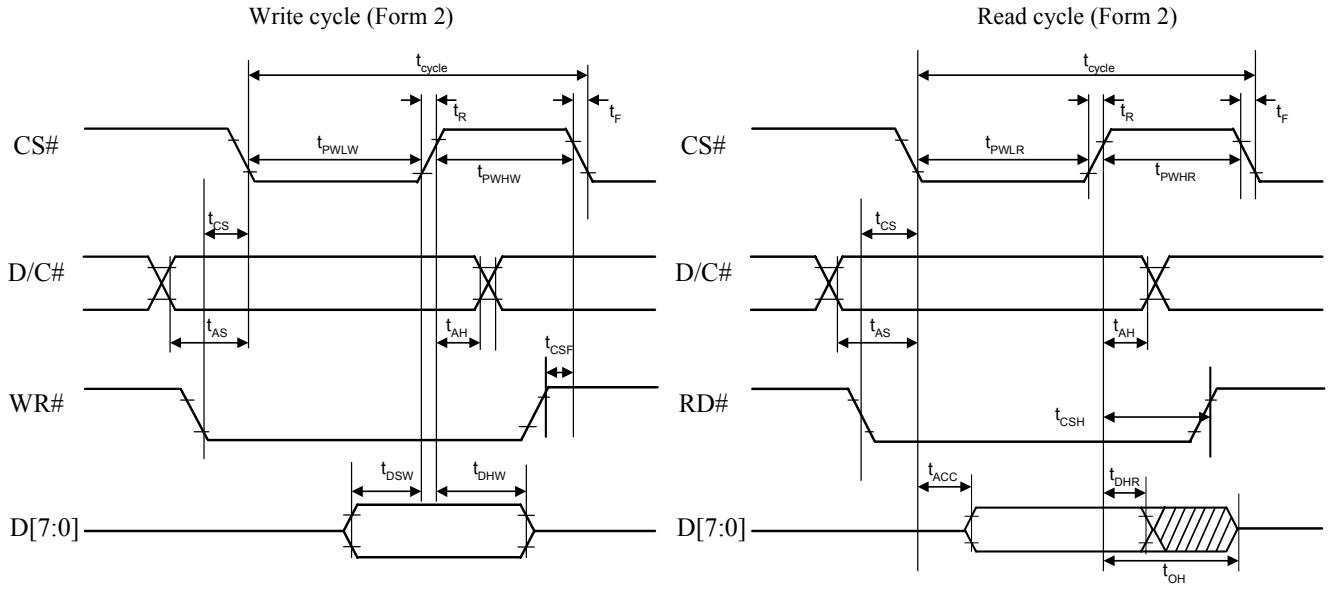
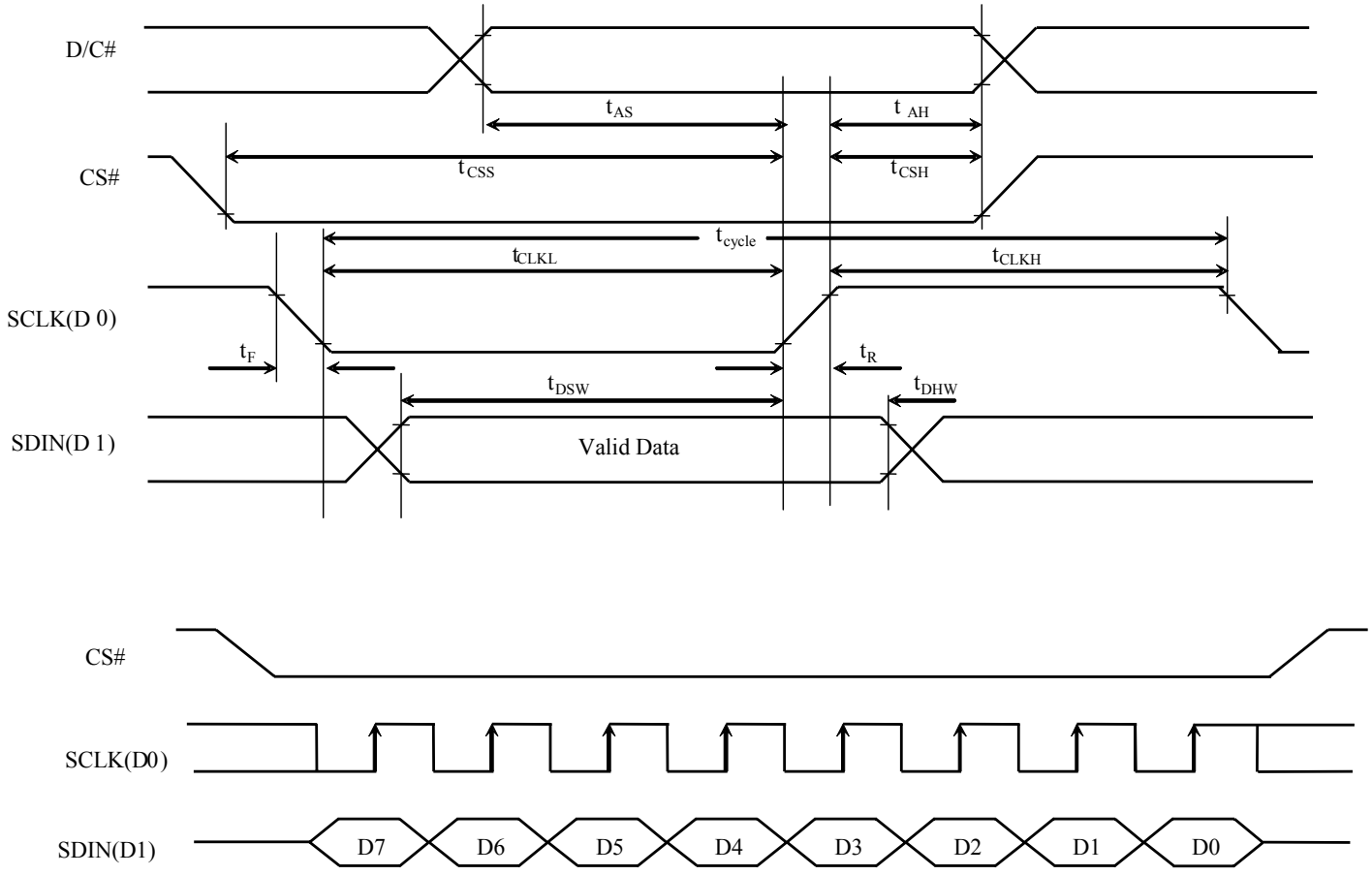


Table 13-4 : Serial Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.3V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 13-4 : Serial interface characteristics



14 Application

Figure 14-1 : Booster Connection Diagram

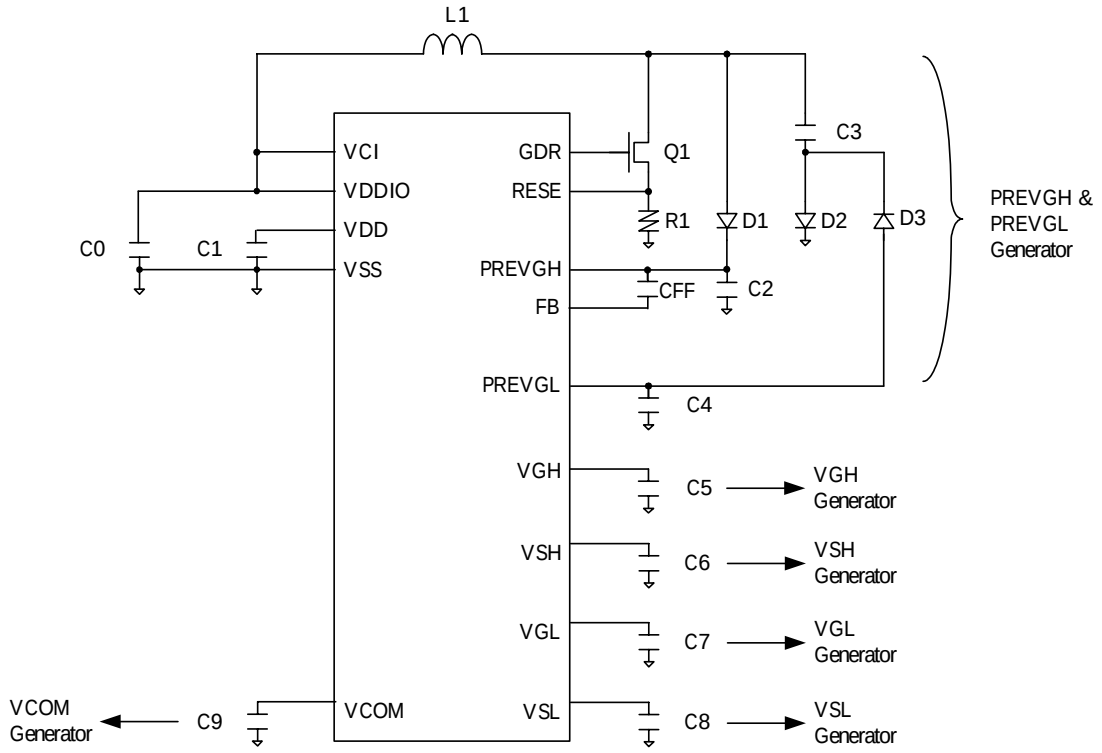


Figure 14-2 : Typical application diagram with SPI interface

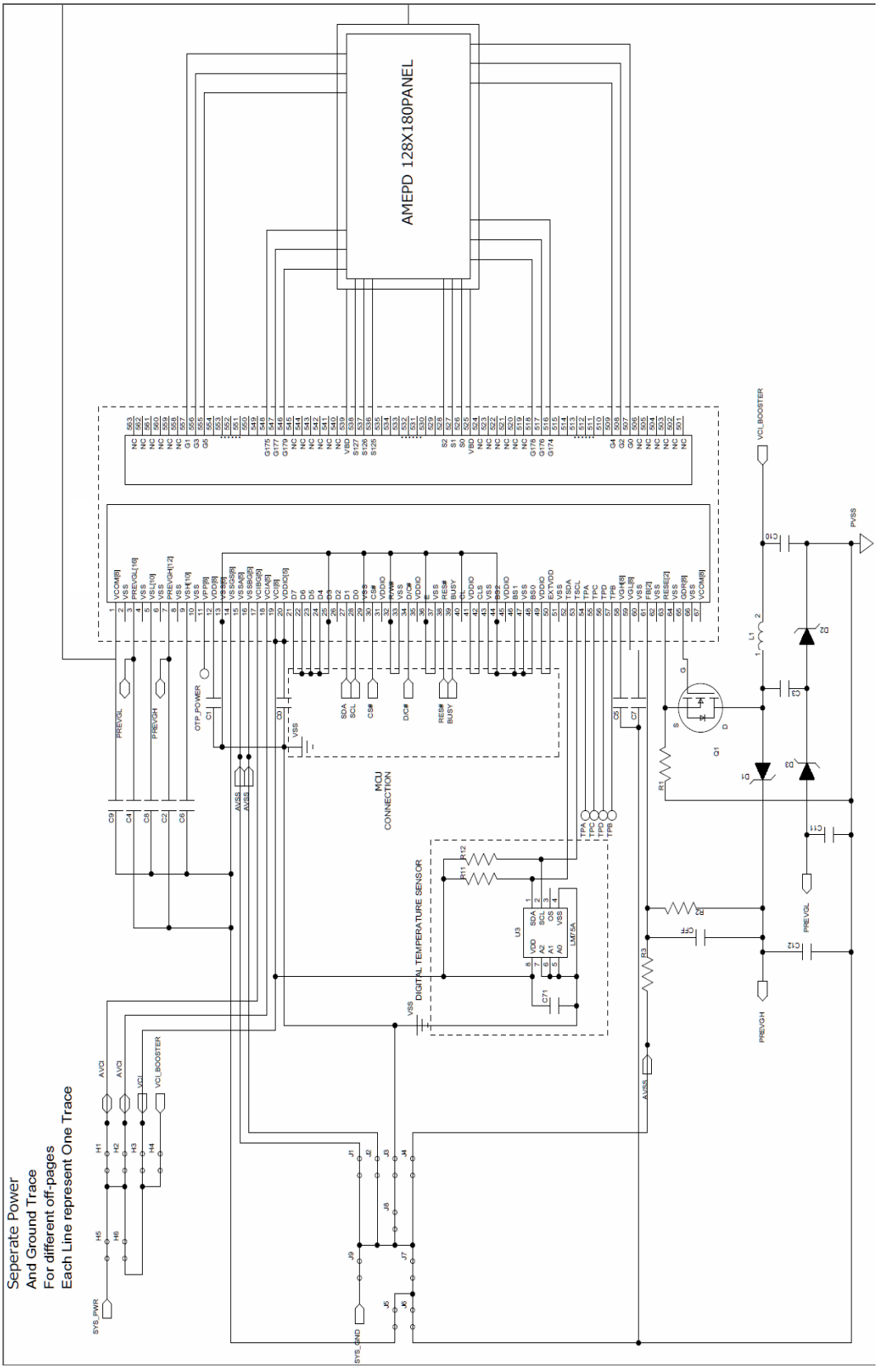


Table 14-1 : Reference Component Value

Part Name	Value	Max Volt. Rating [In V]	Pins Connected	MAX COG ITO resistance [in Ohm]
C0	1uF	6	VCI, VDDIO, VSS	5
C1	1uF	6	VDD, VSS	30
C2	1uF	50	PREVGH	5
C3	4.7uF	50	L1 and D2/D3	NA
C4	1uF	50	PREVGL	5
C5	1uF	25	VGH	10
C6	1uF	25	VSH	5
C7	1uF	25	VGL	10
C8	1uF	25	VSL	5
C9	1uF	6	VCOM	5
C10	10uF	6	VCI [Booster]	NA
C11	4.7uF	50	PREVGL [Booster]	NA
C12	1uF	50	PREVGH [Booster]	NA
C71	1uF	6	VCI [LM75A]	NA
L1	10uH			
Q1	NMOS [Vishay: Si1304BDL]		GDR, RESE	5
D1	Diode [OnSemi: MBR0530]		PREVGH	NA
D2	Diode [OnSemi: MBR0530]			NA
D3	Diode [OnSemi: MBR0530]		PREVGL, VSS	NA
R1	0.47 Ohm		RESE	5
R2	NC		PREVGH, FB	NA
R3	NC		FB, VSS	NA
R11	2.2kOhm			NA
R12	2.2kOhm			NA
U3	LM75A			NA

The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard SJ/T 11363-2006 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)”. Hazardous Substances test report is available upon request.

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