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CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS

MODEL NO . :

E U - K S 0 0 6 6

FOR MESSRS :

CUSTOMER'S APPROVAL

DATE :

BY :

EMERGING DISPLAY TECHNOLOGIES CORPORATION	MODEL NO. E U - K S 0 0 6 6	VERSION 5

RECORDS OF REVISION

DOC. FIRST ISSUE MAY.26 ,1995

DATE	REVISED PAGE NO.	SUMMARY
AUG.02,1995	ALL	APPEND TIMING OF UMC'S UM3881B
APR.15,1996	5~30	APPEND PAGE 5. 3.4 POWER SUPPLY CONDITIONS USING INTERNAL RESET CIRCUIT.
MAR.17,1999	24~31	CHANGED " ROM CODE "
OCT.29,1999	2	3. ELECTRICAL CHARACTERISTICS ADD 3.1.1 DC CHARACTERISTICS FOR KS0066(VDD=2.7V~4.5V) 3.2 AC TIMING CHARACTERISTICS ADD 3.2.2 FOR KS0066(VDD=2.7V~4.5V)

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1. DESCRIPTION

The KS0066(for controller IC KS0066,UM3881,SED1278) dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8- bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

The KS0066 character generator ROM is extended to generate 192 5 x 8 dot character fonts and 32 5 x 10 dot character fonts for a total of 224 different character fonts.

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	VALUE	UNIT
POWER SUPPLY VOLTAGE (1)	V_{DD}-GND	-0.3 TO +7.0	V
POWER SUPPLY VOLTAGE (2)	V_O-GND	V_{DD}-13.5 ~ V_{DD}+0.3	V
INPUT VOLTAGE	V_I	-0.3 TO V_{DD}+0.3	V

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

3. ELECTRICAL CHARACTERISTICS

3.1 DC CHARACTERISTICS FOR SED1278,UM3881,KS0066(VDD=4.5V~5.5V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
OPERATING VOLTAGE	V_{DD}	4.5	5.0	5.5	V	
INPUT HIGH VOLTAGE	V_{IH1}	2.2	—	V_{DD}	V	
INPUT LOW VOLTAGE	V_{IL1}	-0.3	—	0.6	V	
OUTPUT HIGH VOLTAGE(1) (DB0-DB7)	V_{OH1}	2.4	—	—	V	$-I_{OH}$ = 0.205 mA
OUTPUT LOW VOLTAGE (1) (DB0-DB7)	V_{OL1}	—	—	0.4	V	I_{OL} = 1.2 mA
INPUT LEAKAGE CURRENT	I_{L1}	-1	—	1	μA	V_{IN} = 0 TO V_{DD}
PULL-UP MOS CURRENT (DB0-DB7 , RS , R/$\overline{W}$)	$-I_P$	50	125	250	μA	V_{DD} = 5 V
POWER SUPPLY CURRENT	I_{CC}	—	0.35	0.60	mA	Rf OSCILLATION EXTERNAL CLOCK V_{DD}=5V fosc=270KHZ

3.1.1 DC CHARACTERISTICS FOR KS0066(VDD=2.7V~4.5V)

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
OPERATING VOLTAGE	V_{DD}	2.7	—	4.5	V	
INPUT HIGH VOLTAGE	V_{IH1}	0.7*VDD	—	V_{DD}	V	
INPUT LOW VOLTAGE	V_{IL1}	-0.3	—	0.55	V	
OUTPUT HIGH VOLTAGE(1) (DB0-DB7)	V_{OH1}	0.75*VDD	—	—	V	$-I_{OH}$ = 0.1 mA
OUTPUT LOW VOLTAGE (1) (DB0-DB7)	V_{OL1}	—	—	0.2*VDD	V	I_{OL} = 0.1 mA
INPUT LEAKAGE CURRENT	I_{L1}	-1	—	1	μA	V_{IN} = 0 TO V_{DD}
PULL-UP MOS CURRENT (DB0-DB7 , RS , R/$\overline{W}$)	$-I_P$	10	50	120	μA	V_{DD} = 3 V
POWER SUPPLY CURRENT	I_{CC}	—	0.15	0.3	mA	Rf OSCILLATION EXTERNAL CLOCK V_{DD}=3V fosc=270KHZ

3.2 AC TIMING CHARACTERISTICS

3.2.1 FOR SED1278,KS0066(VDD=4.5V~5.5V)

WRITE OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	500	—	—	ns	FIGURE 1
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	220	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	T_{as}	40	—	—	ns	
ADDRESS HOLD TIME	T_{ah}	10	—	—	ns	
DATA SET-UP TIME	T_{dsw}	60	—	—	ns	
DATA HOLD TIME	T_h	10	—	—	ns	

READ OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	500	—	—	ns	FIGURE 2
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	220	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	T_{as}	40	—	—	ns	
ADDRESS HOLD TIME	T_{ah}	10	—	—	ns	
DATA DELAY TIME	T_{ddr}	60	—	120	ns	
DATA HOLD TIME	T_{dhr}	20	—	—	ns	

3.2.2 FOR KS0066(VDD=2.7V~4.5V)

WRITE OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	1000	—	—	ns	FIGURE 1
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	450	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	T_{as}	60	—	—	ns	
ADDRESS HOLD TIME	T_{ah}	20	—	—	ns	
DATA SET-UP TIME	T_{dsw}	195	—	—	ns	
DATA HOLD TIME	T_h	10	—	—	ns	

READ OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	1000	—	—	ns	FIGURE 2
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	450	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	T_{as}	60	—	—	ns	
ADDRESS HOLD TIME	T_{ah}	20	—	—	ns	
DATA DELAY TIME	T_{ddr}	—	—	360	ns	
DATA HOLD TIME	T_{dhr}	5	—	—	ns	

3.2.3 FOR UM3881

WRITE OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	500	—	—	ns	FIGURE 1
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	300	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	t_{AS}	60	—	—	ns	8bit OPERATION MODE
		100	—	—	ns	4bit OPERATION MODE
ADDRESS HOLD TIME	t_{AH}	10	—	—	ns	
DATA SET-UP TIME	t_{DSW}	100	—	—	ns	
DATA HOLD TIME	t_H	10	—	—	ns	

READ OPERATION

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
ENABLE CYCLE TIME	t_{cycE}	500	—	—	ns	FIGURE 2
ENABLE PULSE WIDTH (HIGH LEVEL)	PW_{EH}	300	—	—	ns	
ENABLE RISE/FALL TIME	t_{Er} , t_{Ef}	—	—	25	ns	
ADDRESS SET-UP TIME (RS , R/$\overline{W}$ TO E)	t_{AS}	60	—	—	ns	8bit OPERATION MODE
		100	—	—	ns	4bit OPERATION MODE
ADDRESS HOLD TIME	t_{AH}	10	—	—	ns	
DATA DELAY TIME	t_{DDR}	—	—	190	ns	
DATA HOLD TIME	t_{DHR}	20	—	—	ns	

3.3 TIMING CHARACTERISTICS

3.3.1 WRITE OPERATION

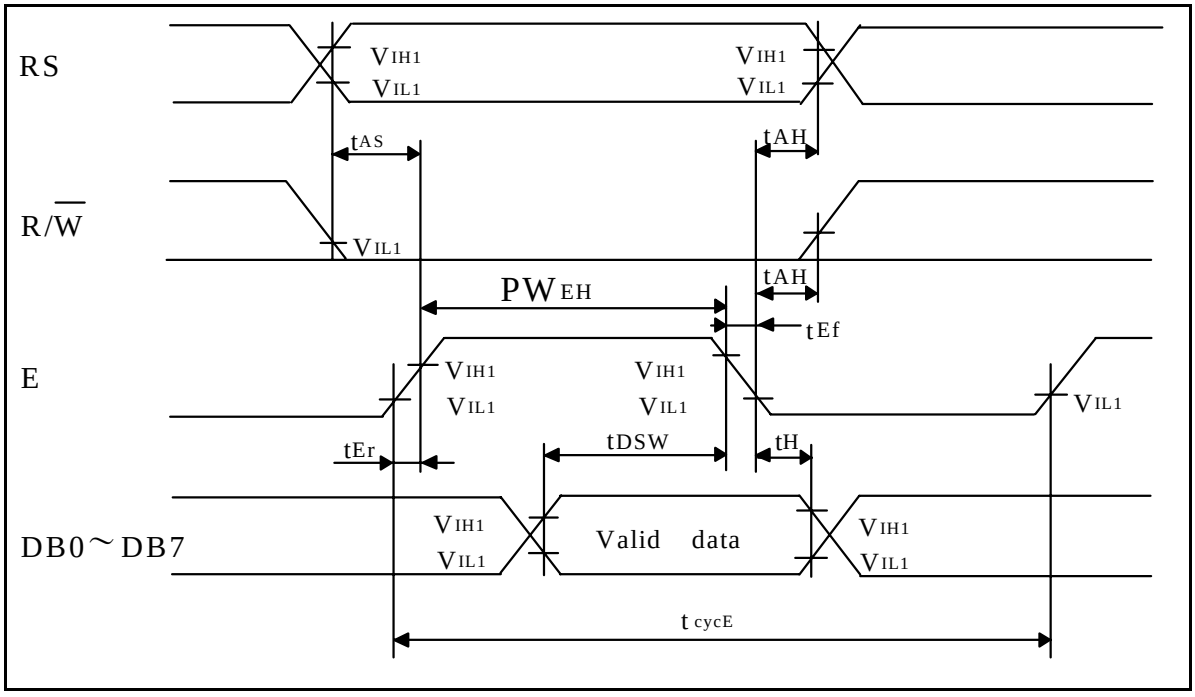


FIGURE 1 WRITE OPERATION

3.3.2 READ OPERATION

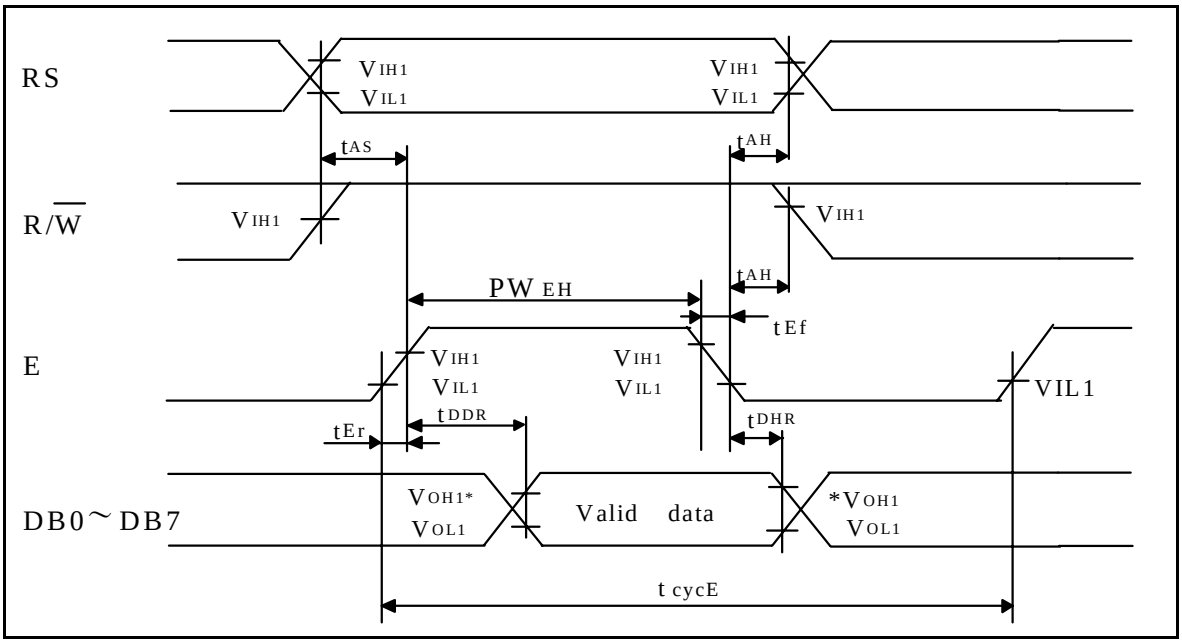
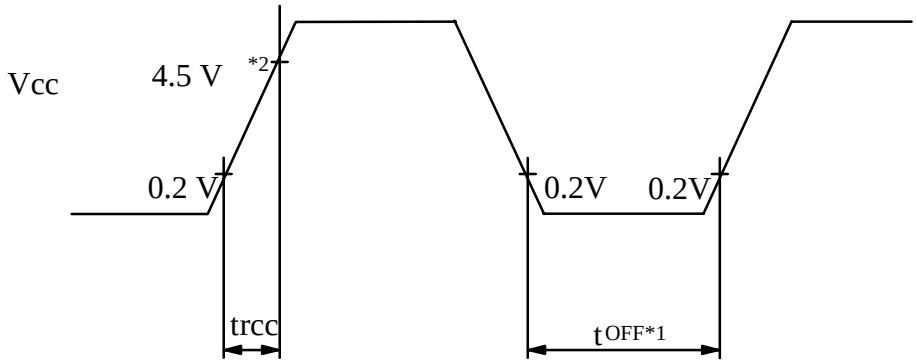


FIGURE 2 READ OPERATION

3.4 POWER SUPPLY CONDITIONS USING INTERNAL RESET CIRCUIT

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
POWER SUPPLY RISE TIME	t_{rCC}	0.1	—	10	ms
POWER SUPPLY OFF TIME	t_{OFF}	1	—	—	ms



0.1 ms ≤ t_{rcc} ≤ 10 ms t_{OFF} ≥ 1 ms

Note : 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5V for Vcc=5v operation.
3. For if 4.5V is not reached during 5V operation, the internal reset circuit will not operate normally.
In this case, the LSI must be initialized by software.
(Refer to the initializing by instruction section.)

4. INTERFACING TO THE MPU

The KS0066 can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPUs.

* For 4-bit interface data, only four bus lines (DB_4 to DB_7) are used for transfer. Bus lines DB0 to DB3 are disabled. The data transfer between the KS0066 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB_4 to DB_7) are transferred before the four low order bits (for 8-bit operation, DB_0 to DB_3)

The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

* For 8-bit interface data, all eight bus lines (DB_0 to DB_7) are used.

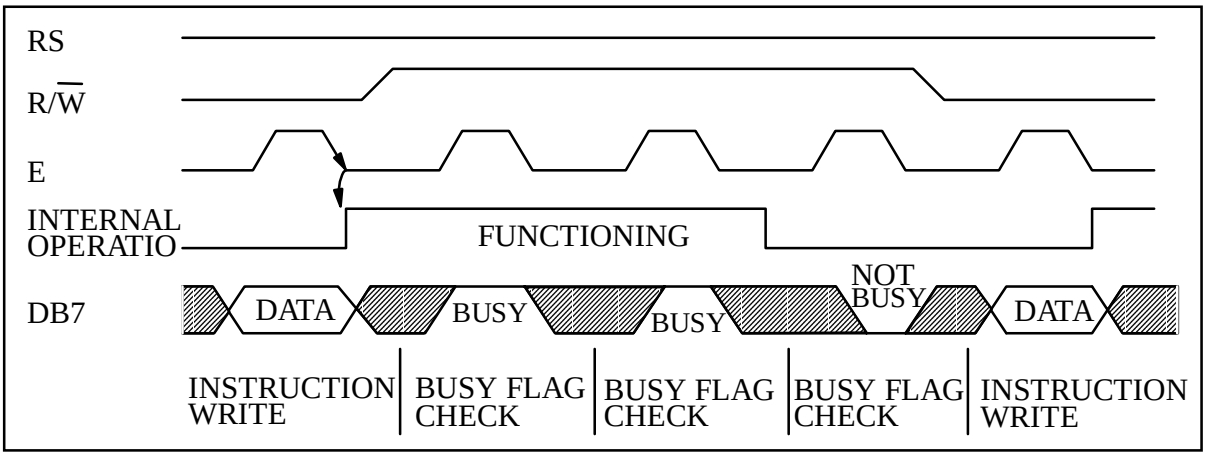


FIGURE 3 EXAMPLE OF BUSY FLAG CHECK TIMING SEQUENCE

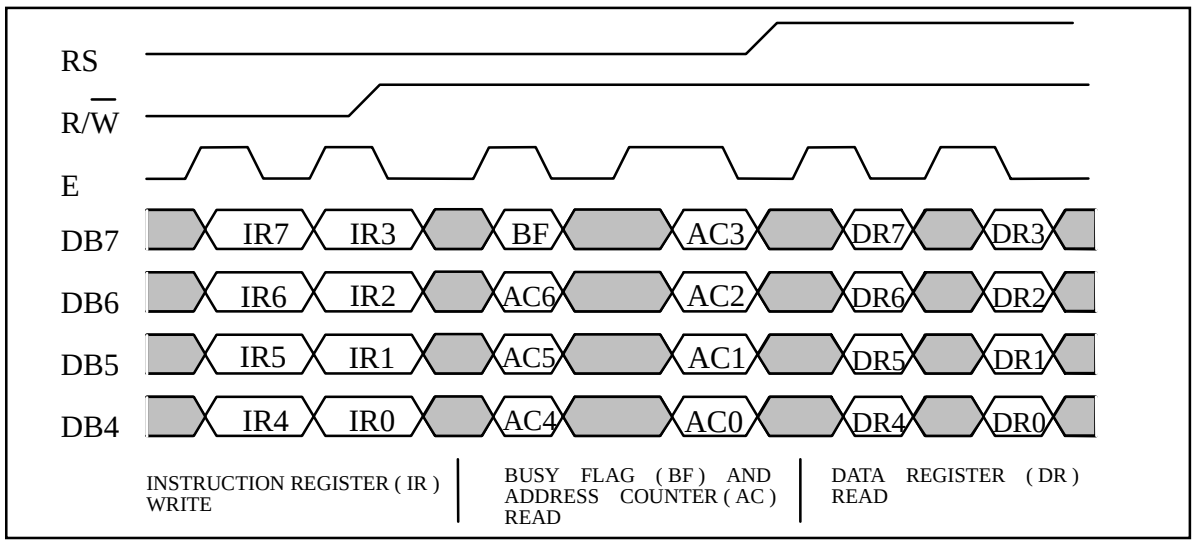
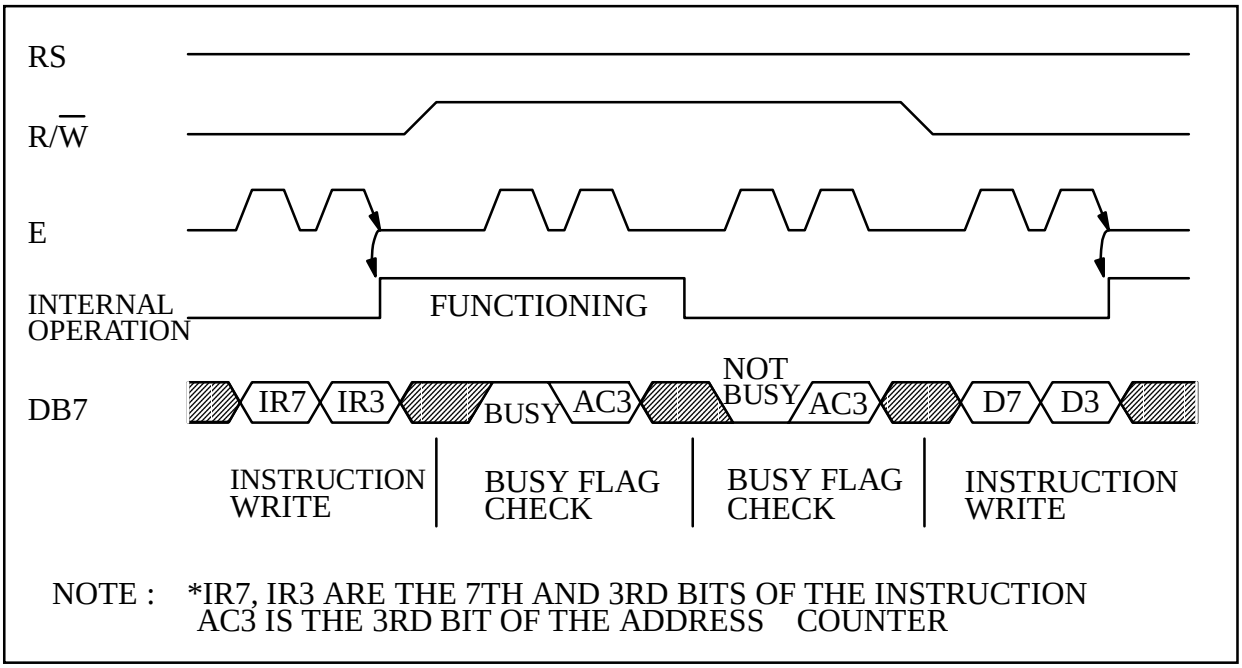


FIGURE 4 4-BIT TRANSFER EXAMPLE



NOTE : *IR7, IR3 ARE THE 7TH AND 3RD BITS OF THE INSTRUCTION
AC3 IS THE 3RD BIT OF THE ADDRESS COUNTER

FIGURE 5 EXAMPLE OF 4-BIT DATA TRANSFER TIMING SEQUENCE

5. RESET FUNCTION

INITIALIZING BY INTERNAL RESET CIRCUIT

An internal reset circuit automadtically initializes the KS0066 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 10 ms after Vcc rises to 4.5 V.

1. Display clear
2. Function set :
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5 x 8 dot character font
3. Display on/off control :
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set :
   I/D = 1; Increment by 1
   S = 0; No shift

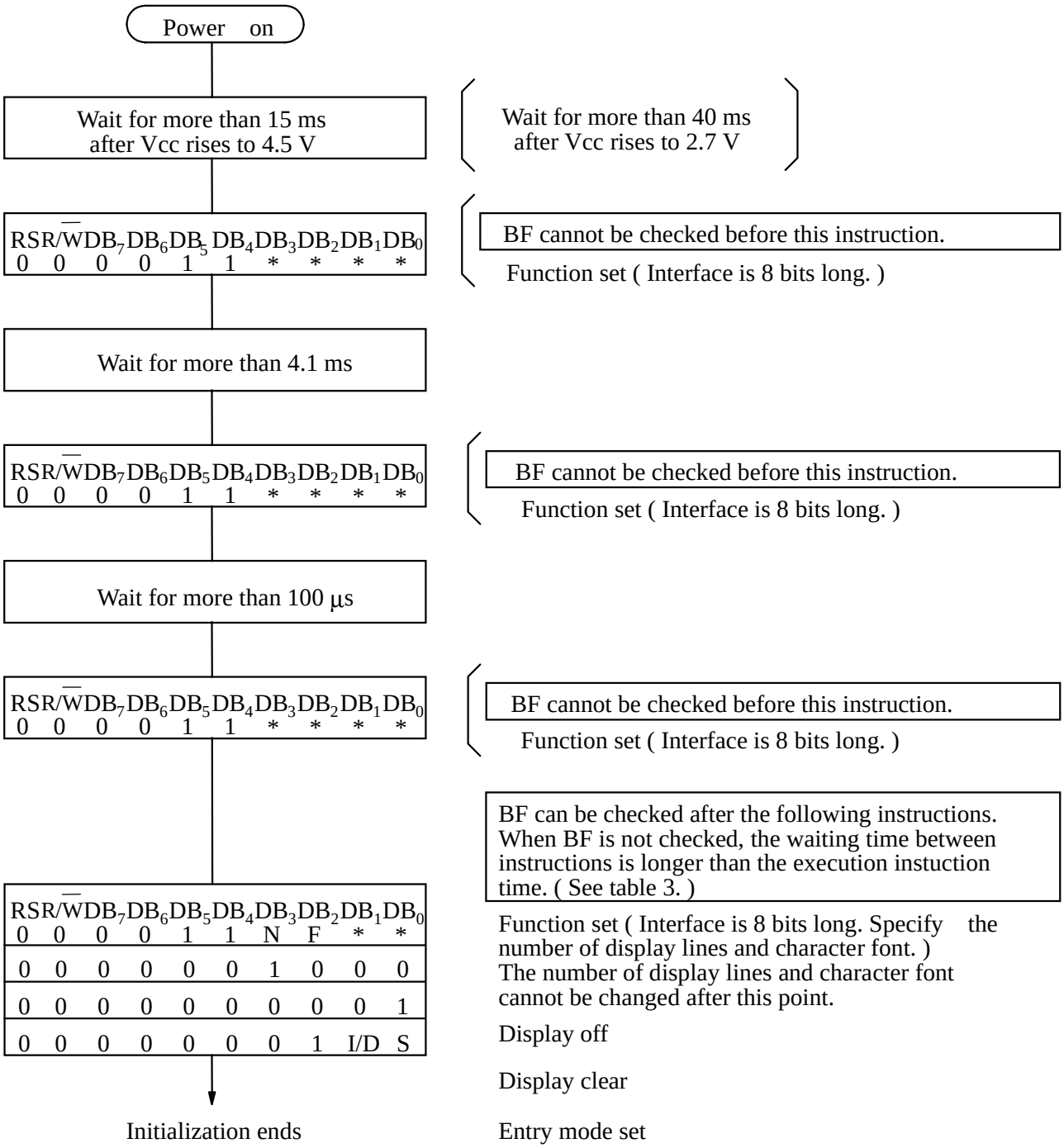
Note : If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the KS0066. For such a case, initialization must be performed by the MPU as explained in the section, Initializing by Instruction.

6. INITIALIZING BY INSTRUCTION

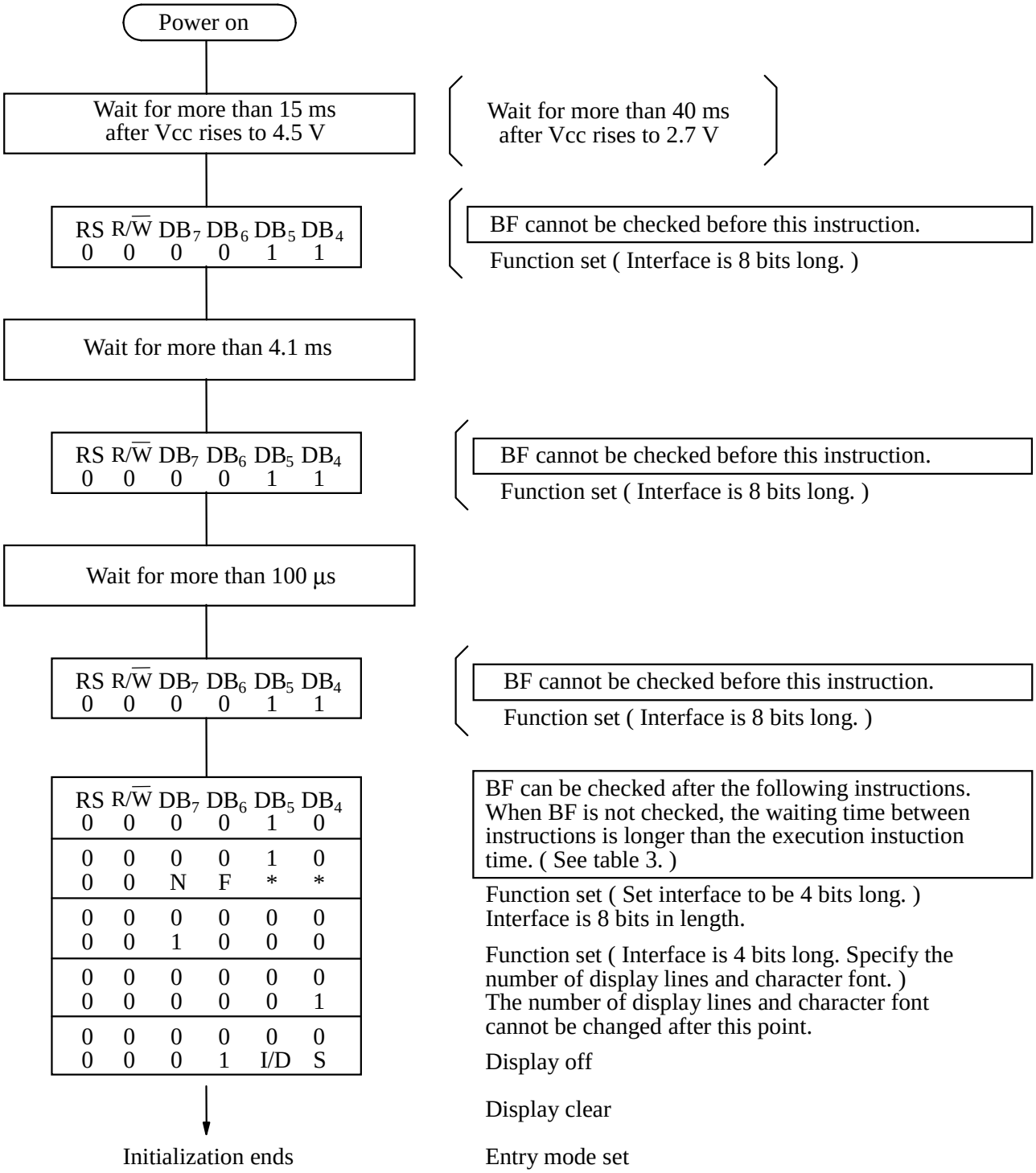
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instructions becomes necessary.

Refer to 6-1 and 6-2 for the procedures on 8-bit and 4-bit initializations, respectively.

6-1 8-BIT INTERFACE



6-2 4-BIT INTERFACE



7. INSTRUCTION DESCRIPTION

OUTLINE

Only the instruction register (IR) and the data register (DR) of the KS0066 can be controlled by the MPU. Before starting the internal operation of the KS0066, control information is temporarily stored into these registers to allow interfacing with various MPUs, which operate at different speeds, or various peripheral control devices. The internal operation of the KS0066 is determined by signals sent from the MPU. These signals, which include register selection signal (RS), read/write signal ($\overline{R/W}$), and the data bus (DB_0 to DB_7), make up the KS0066 instructions (table 1). There are four categories of instructions that :

- Designate KS0066 functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform miscellaneous functions

Normally, instructions that perform data transfer with internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal KS0066 RAM addresses after each data write can lighten the program load of the MPU. Since the display shift instruction (table 1) can perform concurrently with display data write, the user can minimize system development time with maximum programming efficiency.

When an instruction is being executed for internal operation, no instruction other than the busy flag/address read instruction can be executed.

Because the busy flag is set to 1 while an instruction is being executed, check it to make sure it is 0 before sending another instruction from the MPU.

Note : Be sure the KS0066 is not in the busy state (BF = 0) before sending an instruction from the MPU to the KS0066. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to table 3 for the list of each instruction execution time.

CLEAR DISPLAY

		RS	$\overline{R/W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Clear display	Code	0	0	0	0	0	0	0	0	0	1

Clear display writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DD RAM addresses. It then sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. In other words, the display disappears and the cursor or blinking goes to the left edge of the display (in the first line if 2 lines are displayed). It also sets I/D to 1 (increment mode) in entry mode. S of entry mode does not change.

RETURN HOME

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Return home	Code	0	0	0	0	0	0	0	0	1	*

Note :*Don't care.

Return home sets DD RAM address 0 into the address counter, and returns the display to its original status if it was shifted. The DD RAM contents do not change.

The cursor or blinking go to the left edge of the display (in the first line if 2 lines are displayed).

ENTRY MODE SET

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Entry mode set	Code	0	0	0	0	0	0	0	1	I/D	S

I/D：Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from DD RAM.

The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S：Shift the entire display either to the right (I/D = 0) or to the left (I/D = 1) when S is 1. The display does not shift if S is 0.

If S is 1, it will seem as if the cursor does not move but the display does. The display does not shift when reading from DD RAM. Also, writing into or reading out from CG RAM does not shift the display.

DISPLAY ON/OFF CONTROL

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Display on/off control	Code	0	0	0	0	0	0	1	D	C	B

D：The display is on when D is 1 and off when D is 0. When off, the display data remains in DD RAM, but can be displayed instantly by setting D to 1.

C：The cursor is displayed when C is 1 and not displayed when C is 0. Even if the cursor disappears, the function of I/D or other specifications will not change during display data write. The cursor is displayed using 5 dots in the 8th line for 5 x 8 dot character font selection and in the 11th line for the 5 x 10 dot character font selection (figure 6).

B：The character indicated by the cursor blinks when B is 1 (figure 6). The blinking is displayed as switching between all blank dots and displayed characters at a speed of 409.6-ms intervals when fcp or fosc is 250 kHZ. The cursor and blinking can be set to display simultaneously. (The blinking frequency changes according to fosc or the reciprocal of fcp. For example, when fcp is 270 kHZ, 409.6 x 250 / 270 = 379.2 ms.)

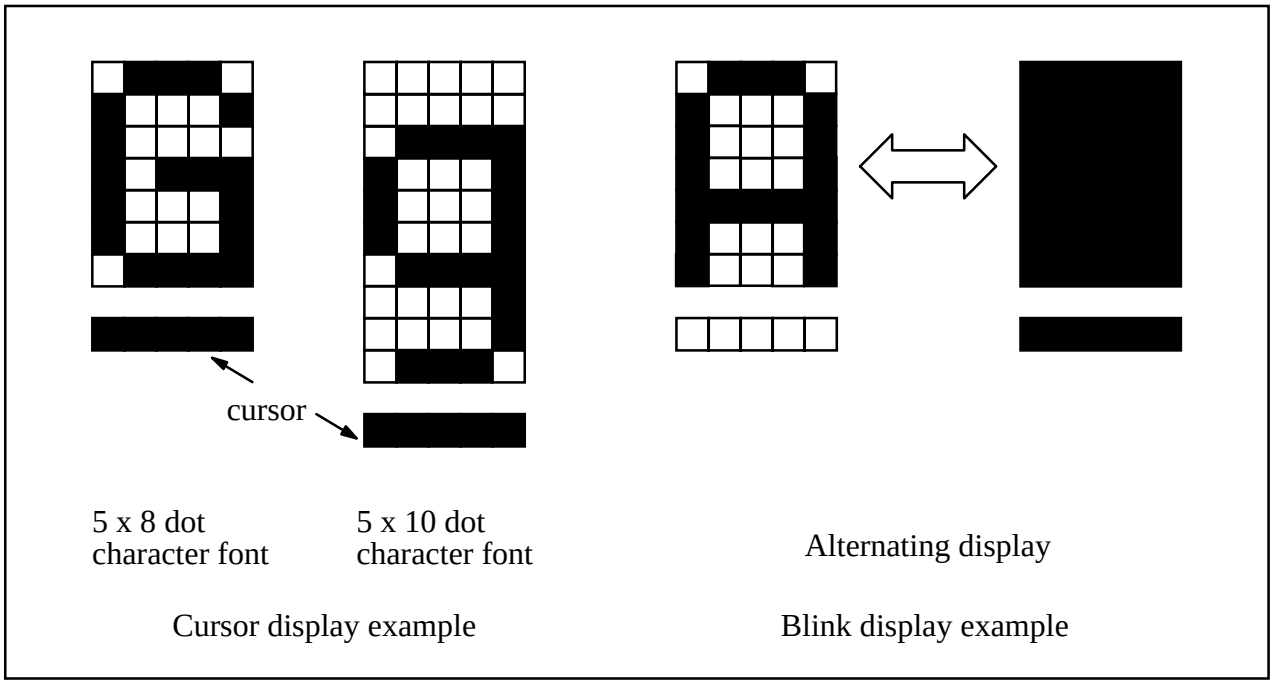


FIGURE 6 CURSOR AND BLINKING

CURSOR OR DISPLAY SHIFT

Cursor or display shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

Note : * Don't care.

Cursor or display shift shifts the cursor position or display to the right or left without writing or reading display data (table 1). This function is used to correct or search the display. In a 2-line display, the cursor moves to the second line when it passes the 40th digit of the first line. Note that the first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly each line moves only horizontally. The second line display does not shift into the first line position.

The address counter (AC) contents will not change if the only action performed is a display shift.

TABLE 1 SHIFT FUNCTION

S/C	R/L	
0	0	SHIFTS THE CURSOR POSITION TO THE LEFT. (AC IS DECREMENTED BY ONE.)
0	1	SHIFTS THE CURSOR POSITION TO THE RIGHT. (AC IS INCREMENTED BY ONE.)
1	0	SHIFTS THE ENTIRE DISPLAY TO THE LEFT. THE CURSOR FOLLOWS THE DISPLAY SHIFT.
1	1	SHIFTS THE ENTIRE DISPLAY TO THE RIGHT. THE CURSOR FOLLOWS THE DISPLAY SHIFT.

FUNCTION SET

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Function set	Code	0	0	0	0	1	DL	N	F	*	*	Note : * Don't care.

DL : Sets the interface data length. Data is sent or received in 8-bit lengths (DB_7 to DB_0) when DL is 1, and in 4-bit lengths (DB_7 to DB_4) when DL is 0.

When 4-bit length is selected, data must be sent or received twice.

N : Sets the number of display lines.

F : Sets the character font.

Note : Perform the function at the head of the program before executing any instructions (except for the read busy flag and address instruction). From this point, the function set instruction cannot be executed unless the interface data length is changed.

TABLE 2 FUNCTION SET

N	F	NO. OF DISPLAY LINES	CHARACTER FONT	DUTY FACTOR	REMARKS
0	0	1	5 X 8 DOTS	1/8	
0	1	1	5 X 10 DOTS	1/11	
1	*	2	5 X 8 DOTS	1/16	CANNOT DISPLAY TWO LINES FOR 5 X 10 DOT CHARACTER FONT

Note : * Indicates don't care.

SET CG RAM ADDRESS

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Set CG RAM address	Code	0	0	0	1	A	A	A	A	A	A

Higher order bit ← → Lower order bit

Set CG RAM address sets the CG RAM address binary AAAAAA into the address counter.

Data is then written to or read from the MPU for CG RAM.

SET DD RAM ADDRESS

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Set DD RAM address	Code	0	0	1	A	A	A	A	A	A	A

Higher order bit ← → Lower order bit

Set DD RAM address sets the DD RAM address binary AAAAAAA into the address counter.

Data is then written to or read from the MPU for DD RAM.

However, when N is 0 (1-line display), AAAAAAA can be 00H to 4FH. When N is 1 (2-line display), AAAAAAA can be 00H to 27H for the first line, and 40H to 67H for the second line.

READ BUSY FLAG AND ADDRESS

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Read busy flag and address	Code	0	1	BF	A	A	A	A	A	A	A

Higher order bit ← → Lower order bit

Read busy flag and address reads the busy flag (BF) indicating that the system is now internally operating on a previously received instruction. If BF is 1, the internal operation is in progress. The next instruction will not be accepted until BF is reset to 0. Check the BF status before the next write operation. At the same time, the value of the address counter in binary AAAAAAA is read out, This addresses counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. The address contents are the same as for instructions set CG RAM address and set DD RAM address.

WRITE DATA TO CG OR DD RAM

		RS	R/$\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Write data to CG or DD RAM	Code	1	0	D	D	D	D	D	D	D	D

← Higher order bit Lower order bit →

Write data to CG or DD RAM writes 8-bit binary data DDDDDDDD to CG or DD RAM.

To write into CG or DD RAM is determined by the previous specification of the CG RAM or DD RAM address setting. After a write, the address is automatically incremented or decremented by 1 according to the entry mode. The entry mode also determines the display shift.

READ DATA FROM CG OR DD RAM

Read data from CG or DD RAM

Code

RS	$\overline{R/W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	1	D	D	D	D	D	D	D	D

← Higher order bit Lower order bit →

Read data from CG or DD RAM reads 8-bit binary data DDDDDDDD from CG or DD RAM.

The previous designation determines whether CG or DD RAM is to be read. Before entering this read instruction, either CG RAM or DD RAM address set instruction must be executed. If not executed, the first read data will be invalid. When serially executing read instructions, the next address data is normally read from the second read. The address set instructions need not be executed just before this read instruction when shifting the cursor by the cursor shift instruction (when reading out DD RAM). The operation of the cursor shift instruction is the same as the set DD RAM address instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed regardless of the entry mode.

Note : The address counter (AC) is automatically incremented or decremented by 1 after the write instructions to CG RAM or DD RAM are executed. The RAM data selected by the AC cannot be read out at this time even if read instructions are executed. Therefore, to correctly read data, execute either the address set instruction or cursor shift instruction (only with DD RAM), then just before reading the desired data, execute the read instruction from the second time the read instruction is sent.

TABLE 3 INSTRUCTIONS

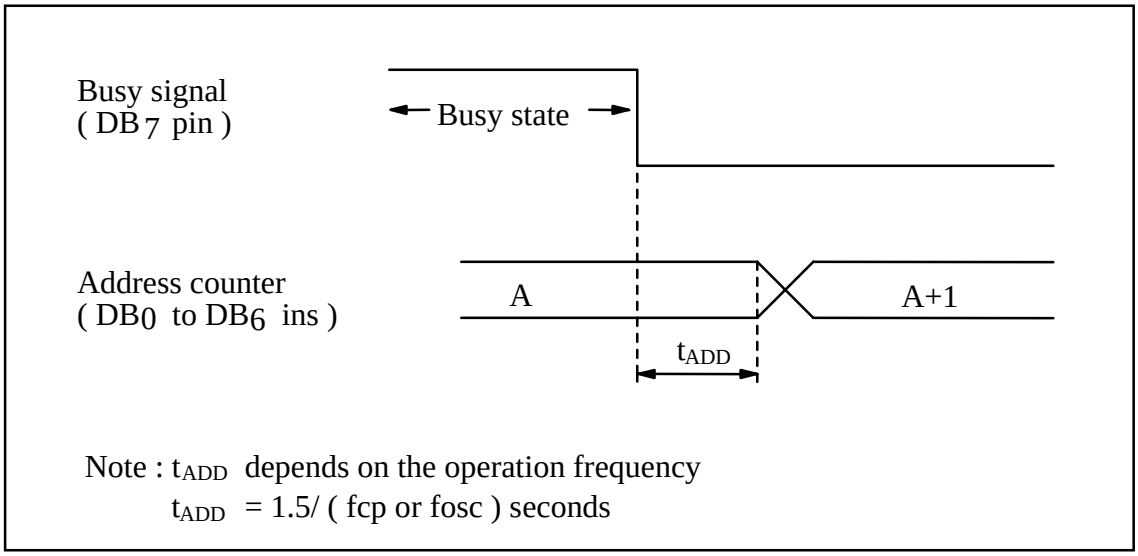
INSTRUCTION	CODE										DESCRIPTION	EXECUTION TIME (MAX) (WHEN fcp OR fosc IS 250 KHZ
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64 ms
Return home	0	0	0	0	0	0	0	0	1	—	Sets DD RAM address 0 in address counter. Also returns display from being shifted to original position. DD RAM contents remain unchanged.	1.64 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	40 μs
Display on/off control	0	0	0	0	0	0	1	D	C	B	Sets entire display (D) on/off, cursor on/off (C), and blinking of cursor position character (B).	40 μs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	—	—	Moves cursor and shifts display without changing DD RAM contents.	40 μs
Function set	0	0	0	0	1	DL	N	F	—	—	Sets interface data length (DL), number of display lines (N), and character font (F).	40μs
Set CG RAM address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CG RAM address CG RAM data is sent and received after this setting.	40 μs
Set DD RAM address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read busy flag & address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 μs

TABLE 3 INSTRUCTIONS (CONT)

INSTRUCTION	CODE										DESCRIPTION	EXECUTION TIME (MAX) (WHEN fcp OR fosc IS 250 KHZ
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Write data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM.	37 μs t_{ADD} = 4μs*
Read data from CG or DD RAM	1	1	Read data								Reads data from DD RAM or CG RAM.	37 μs t_{ADD} = 4μs*
	I/D = 1 : Increment I/D = 0 : Decrement S = 1 : Accompanies display shift S/C= 1 : Display shift S/C= 0 : Cursor move R/L= 1 : Shift to the right R/L= 0 : Shift to the left DL = 1 : 8 bits, DL = 0 : 4 bits N = 1 : 2 lines, N = 0 : 1 line F = 1 : 5 X 10 dots, F = 0 : 5 X 8 dots BF = 1 : Internally operating BF = 0 : Instructions acceptable										DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address (corresponds to cursor address) AC : Address counter used for both DD and CG RAM addresses	

Note :-- indicates no effect.

* After execution of the CG RAM/DD RAM data write or read instruction, the RAM address counter is incremented or decremented by 1. The RAM address counter is updated after the busy flag turns off. In figure 7, t_{ADD} is the time elapsed after the busy flag turns off until the address counter is updated.



Note : t_{ADD} depends on the operation frequency
t_{ADD} = 1.5/ (fcp or fosc) seconds

FIGURE 7 ADDRESS COUNTER UPDATE

8. PROGRAMMING CHARACTER PATTERNS

This section explains the correspondence between addresses and data used to program character patterns in EPROM. The KS0066 character generator ROM can generate 192 5 x 8 dot character patterns and 32 5 x 10 dot character patterns for a total of 224 different character patterns.

EPROM address data and character pattern data correspond with each other to form a 5 x 8 or 5 x 10 dot character pattern (tables 4 and 5)

HANDLING UNUSED CHARACTER PATTERNS

1. EPROM data outside the character pattern area : Always input 0s.

2. EPROM data in CG RAM area : Always input 0s. (Input 0s to EPROM addresses 00H to FFH.)

3. EPROM data used when the user does not use any KS0066 character pattern : According to the user application, handled in one of the two ways listed as follows.

   (1) When unused character patterns are not programmed : If an unused character code is written into DD RAM, all its dots are lit. By not programing a character pattern, all of its bits become lit. (This is due to the EPROM being filled with 1s after it is erased.)

   (2) When unused character patterns are programmed as 0s : Nothing is displayed even if unused character codes are written into DD RAM. (This is equivalent to a space.)

TABLE 4 EXAMPLE OF CORRESPONDENCE BETWEEN EPROM ADDRESS DATA AND CHARACTER PATTERN (5 x 8 DOTS)

EPROM ADDRESS												DATA					
A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_4	O_3	O_2	O_1	LSB O_0	
								0	0	0	0	1	0	0	0	0	
								0	0	0	1	1	0	0	0	0	
								0	0	1	0	1	0	1	1	0	
								0	0	1	1	1	1	0	0	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	1	1	1	1	0	
0	1	1	0	0	0	1	0	0	1	1	1	0	0	0	0	0	← Cursor position
								1	0	0	0	0	0	0	0	0	
								1	0	0	1	0	0	0	0	0	
								1	0	1	0	0	0	0	0	0	
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	
CHARACTER CODE								LINE POSITION									

Note : 1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 9 and the following lines must be blanked with 0s for a 5 x 8 dot character fonts.

TABLE 5 EXAMPLE OF CORRESPONDENCE BETWEEN EPROM ADDRESS DATA AND CHARACTER PATTERN (5 x 10 DOTS)

EPROM ADDRESS												DATA					
																LSB	
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1	O0	
								0	0	0	0	0	0	0	0	0	
								0	0	0	1	0	0	0	0	0	
								0	0	1	0	0	1	1	0	1	
								0	0	1	1	1	0	0	1	1	
								0	1	0	0	1	0	0	0	1	
								0	1	0	1	1	0	0	0	1	
								0	1	1	0	0	1	1	1	1	
0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	0	1	
								1	0	0	0	0	0	0	0	1	
								1	0	0	1	0	0	0	0	1	
								1	0	1	0	0	0	0	0	0	← Cursor position
								1	0	1	1	0	0	0	0	0	
								1	1	0	0	0	0	0	0	0	
								1	1	0	1	0	0	0	0	0	
								1	1	1	0	0	0	0	0	0	
								1	1	1	1	0	0	0	0	0	
CHARACTER CODE								LINE POSITION									

Note: 1. EPROM addresses A_{11} to A_4 correspond to a character code.
2. EPROM addresses A_3 to A_0 specify a line position of the character pattern.
3. EPROM data O_4 to O_0 correspond to character pattern data.
4. EPROM data O_5 to O_7 must be specified as 0.
5. A lit display position (black) corresponds to a 1.
6. Line 11 and the following lines must be blanked with 0s for a 5 x 10 dot character fonts.

TABLE 6 RELATIONSHIP BETWEEN CG RAM ADDRESSES, CHARACTER CODES (DD RAM) AND CHARACTER PATTERNS (CG RAM DATA) FOR 5 x 8 DOT CHARACTER PATTERNS

CHARACTERCODES (DD RAM DATA)	CG RAM ADDRESS	CHARACTER PATTERNS (CG RAM DATA)	
7 6 5 4 3 2 1 0	5 4 3	2 1	7 6 5 4 3 2 1 0	
HIGH LOW	HIGH	LOW	HIGH LOW	
0 0 0 0 * 0 0 0	0 0 0	0 0	* * * 1 1 1 1 0	Character pattern (1)
		0 1	1 0 0 0 1	
		1 0	1 0 0 0 1	
		1 1	1 1 1 1 0	
		0 0	1 0 1 0 0	
		0 1	1 0 0 1 0	
		1 0	1 0 0 0 1	
		1 1	* * * 0 0 0 0 0	Cursor position
0 0 0 0 * 0 0 1	0 0 1	0 0	* * * 1 0 0 0 1	Character pattern (2)
		0 1	0 1 0 1 0	
		1 0	1 1 1 1 1	
		0 0	0 0 1 0 0	
		0 1	1 1 1 1 1	
		1 0	0 0 1 0 0	
		1 1	0 0 1 0 0	
		0 0	* * * 0 0 0 0 0	Cursor position
0 0 0 0 * 1 1 1	1 1 1	0 0	* * *	
		0 1		
		1 0		
		1 1		
		0 0		
		0 1		
		1 0		
		1 1	* * *	

Note : 1. Character code bits 0 to 2 correspond to CG RAM address bits 3 to 5 (3 bits: 8 types).

2. CG RAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with th cursor.
   Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display .

3. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.

4. Character pattern row positions correspond to CG RAM data bits 0 to 4 (bit 4 being at the left).

5. As shown table 6, CG RAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
   1 for CG RAM data corresponds to display selection and 0 to non-selection.
   * Indicates no effect.

TABLE 7 RELATIONSHIP BETWEEN CG RAM ADDRESSES, CHARACTER CODES (DD RAM) AND CHARACTER PATTERNS (CG RAM DATA) (CONT)

FOR 5 x 10 DOT CHARACTER PATTERNS

CHARACTER CODES (DD RAM DATA)	CG RAM ADDRESS	CHARACTE PATTERN (CG RAM DATA)
7 6 5 4 3 2 1 0 HIGH LOW	5 4 3 2 1 0 HIGH LOW	7 6 5 4 3 2 1 0 HIGH LOW
0 0 0 0 * 0 0 *	0 0 0 0 0	* * * 0 0 0 0 0
	0 0 0 1	0 0 0 0 0
	0 0 1 0	1 0 1 1 0
	0 0 1 1	1 1 0 0 1
	0 1 0 0	1 0 0 0 1
0 0	0 1 0 1	1 0 0 0 1
	0 1 1 0	1 1 1 1 0
	0 1 1 1	1 0 0 0 0
	1 0 0 0	1 0 0 0 0
	1 0 0 1	1 0 0 0 0
	1 0 1 0	* * * 0 0 0 0 0
	1 0 1 1	* * * * * * * *
	1 1 0 0	
	1 1 0 1	
	1 1 1 0	
	1 1 1 1	* * * * * * * *
0 0 0 0 * 1 1 *	0 0 0 0	* * *
	0 0 0 1	
1 1	1 0 0 1	
	1 0 1 0	
	1 0 1 1	* * * * *
	1 1 0 0	
	1 1 0 1	
	1 1 1 0	
	1 1 1 1	* * * * * * * *

Character patter

Cursor position

Note : 1. Character code bits 1 and 2 correspond to CG RAM address bits 4 and 5 (2 bits : 4 types).

2. CG RAM address bits 0 to 3 designate the character pattern line position. The 11th line is the cursor position and its display is formed by a logical OR with the cursor.
   Maintain the 11th line data corresponding to the cursor display position at 0 as the cursor display.
   If the 11th line data is “1”, “1” bits will light up the 11th line regardless of the cursor presence.
   Since lines 12 to 16 are not used for display, they can be used for general pattern data RAM.

3. Character pattern row positions are the same as 5 x 8 dot character pattern positions.

4. CG RAM character patterns are selected when character code bits 4 to 7 are all 0.
   However, since character code bits 0 and 3 have no effect, the P display example above can be selected by character codes 00H, 01H, 08H, and 09H.

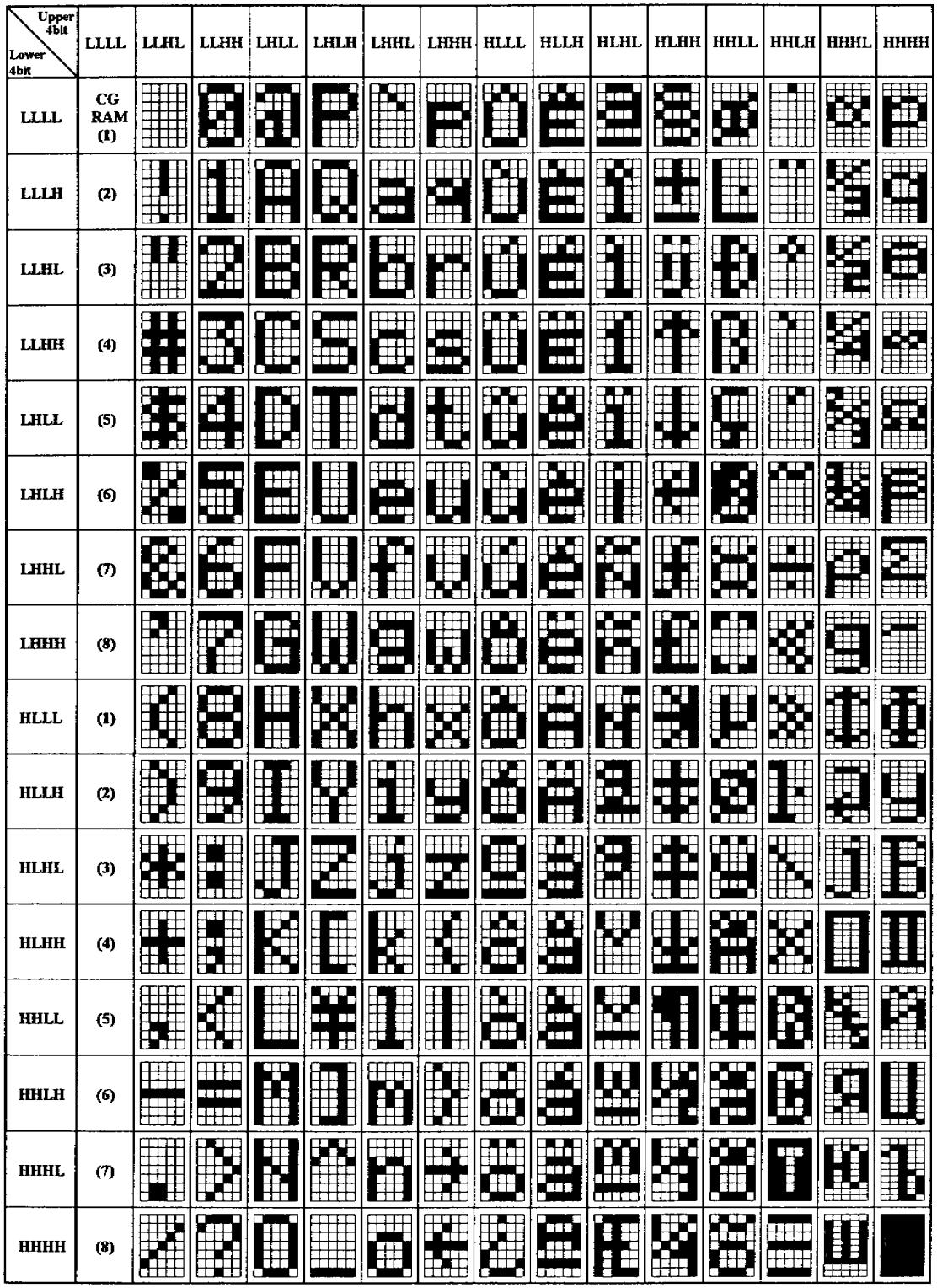
5. 1 for CG RAM data corresponds to display selection and 0 to non-selection.
   * Indicates no effect.

9. CHARACTER CODES AND CHARACTER PATTERNS

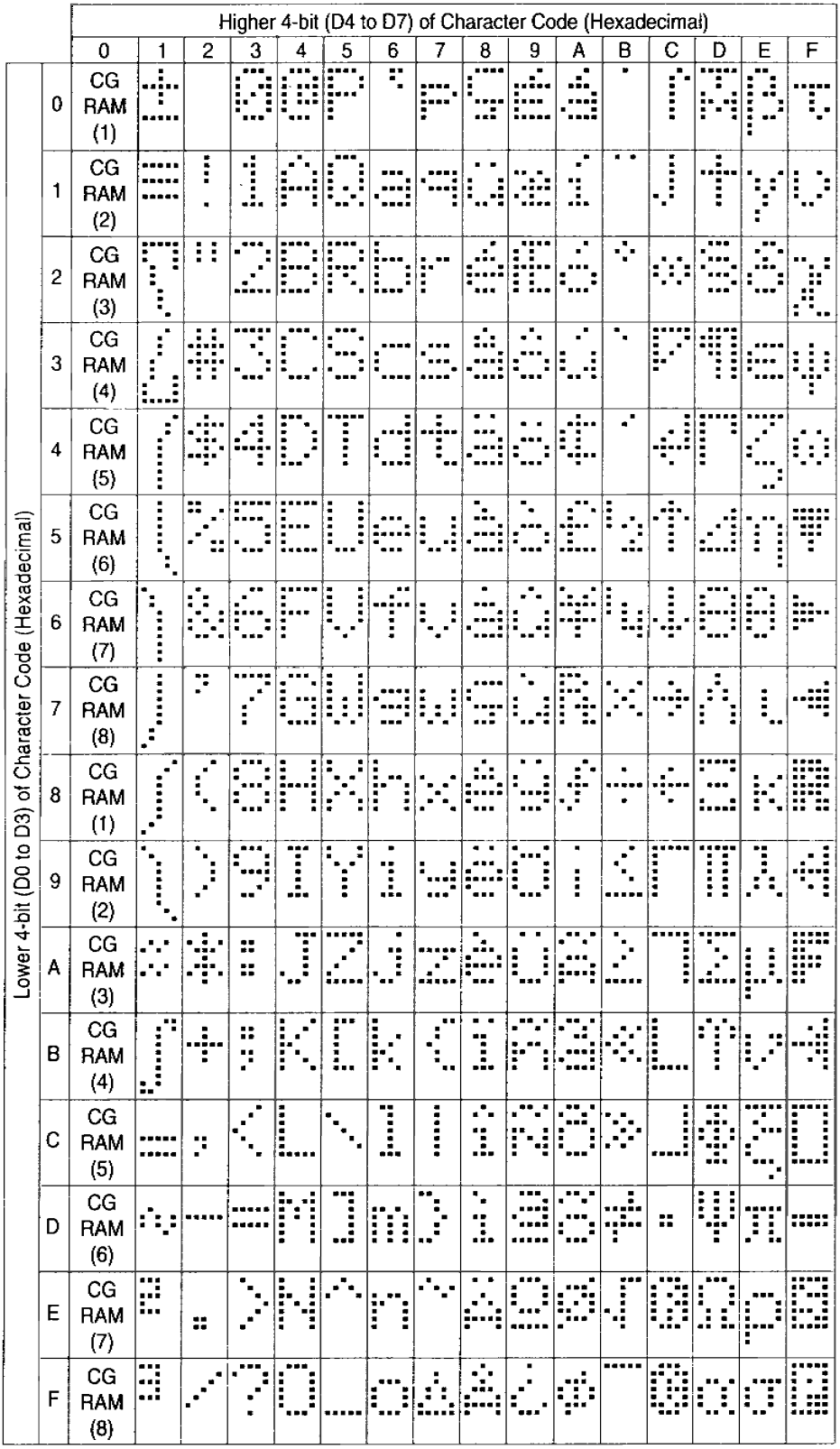
9-1 CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERNS (ROM CODE : KS0066F00 / UM3881-01)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

9-2 CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERNS (ROM CODE : KS0066F05)



9-3 CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERNS (ROM CODE : UM3881-02 / SED1278D0B)



9-4 CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERNS (ROM CODE : SED1278D0H)